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A multi-channel high-speed fiber-optic digital data link

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THESIS

A MULTI-CHANNEL HIGH-SPEED FIBER-OPTIC DIGITAL DATA LINK

by

James H. Mills

December 1996

Thesis Advisor: John P. Powers

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This research presents the design, implementation, and testing of a multi-channel, high-speed fiber-optic data link. The aim of this study is to evaluate this data link for use as a viable and economical shipboard communication system. Incorporated in the design are commercial off-the-shelf technology system (COTS) high-speed fiber-optic modules, standard single-mode optical fiber, and integrated circuits from two digital logic families—Emitter Coupled Logic (ECL) and Transistor-Transistor Logic (TTL). Time division multiplexing (TDM) techniques are used for transmission and reception of the 14-channel data link. The data link is a subsystem of the high-resolution digital antenna system.

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A MULTI-CHANNEL HIGH-SPEED FIBER-OPTIC DIGITAL DATA LINK

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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

This research presents the design, implementation, and testing of a multi-channel, high-speed fiber-optic data link. The aim of this study is to evaluate this data link for use as a viable and economical shipboard communication system. Incorporated in the design are commercial off-the-shelf technology system (COTS) high-speed fiber-optic modules, standard single-mode optical fiber, and integrated circuits from two digital logic families—Emitter Coupled Logic (ECL) and Transistor-Transistor Logic (TTL). Time division multiplexing (TDM) techniques are used for transmission and reception of the high-speed 14-channel data link. The data link is a subsystem of the high-resolution digital antenna system.

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LIST OF ACRONYMNS

ADC. Analog to Digital Converter.

BLL. Buffer Line Logic.

BPS. Bits per second. (K: thousand; M: million; G: billion)

C4I. Command, Control, Communications, Computers, and Intelligence.

COTS. Commercial Off-the-shelf Technology Systems.

ECL. Emitter Coupled Logic.

EMC. Electromagnetic Compatibility.

EMI. Electromagnetic Interference.

ESD. Electro-Static Discharge.

LSI. Large Scale Integration.

MECL. Motorola Emitter Coupled Logic.

MTBF. Mean Time Between Failure.

MTTF. Mean Time to Failure.

MTTR. Mean Time to Repair.

OTDM. Optical Time Division Multiplexing.

PLL. Phase Locked Loop.

RF. Radio Frequency.

RX. Receiver.

TDM. Time Division Multiplexing.

TTL. Transistor-Transistor Logic.

TX. Transmitter.

VLSI. Very Large Scale Integration.

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I. INTRODUCTION

A. PURPOSE OF STUDY AND BENEFITS

In the age of the downsized Navy and increased littoral operations, the Navy's demand for high-speed, high-bandwidth command, control, communications, computers and intelligence (C4I) systems has never been greater. When analyzing the amount of data a major combatant must receive and process, it can easily be argued that such high-speed, high-bandwidth systems are vital to attain dominance of the battle space. In an effort to find a cost-effective and capable data link for the warfighter, a high-speed, multi-channel optoelectronic data link, as presented in this thesis, is proposed to meet these requirements. The viability of developing such a data link using commercial off-the-shelf technology system (COTS) components vice using prohibitively expensive specialized *military-only* components was investigated in this thesis research. By integrating traditional and high-speed microelectronic circuitry along with optical fiber, the data link achieves the necessary high throughput. With such a data link comes the added benefits of increased link security, increased weight and space savings, improved EMI and EMC performance, and better system reliability.

B. DATA LINK CONCEPTS

The purpose of a data link is to convey information (the data) from a source to a receiver using a readily available and efficient transmission medium (the link). Modern communication systems typically uses the following media for data transmission: copper media (i.e., twisted pair and coaxial cable), optical fiber, or wireless media (i.e., visual communication, microwave, satellite, or other RF frequency ranges) [Reference 1]. A comparison of different transmission media and the electromagnetic spectrum is described in Table 1.1 and Figure 1.1. In naval communications, both the physical distance between units and the mobile nature of the platforms typically preclude the use of physical

connection media (copper and optical fiber) between units. Thus, the use of wireless transmission media is required. Most communications will require the use of an antenna to receive and transmit the information via electromagnetic waves.

	Twisted Pair	Coaxial Cable	Optical Fiber	ELF,VF,LF, HF,VHF,UHF	Microwave	Satellite (SHF, EHF)
Data Rate	1-2 Mbps at 1 mi 2.4 Kbps at 10 mi	10 Mbps is typical	500 Mbps typical. Gbps rate too.	Ranges between 0.003 bps to 115.2 kbps	200-300 Mbps	1-2 Mbps
Susceptibility to interference	EMI and crosstalk are problems	Shielding reduces much interference	Immune to most interference	Many EMI and EMC problems	Solid objects cause problems.	Atmospheric interference is a problem.
Distance	Up to 10 mi with lower data rates	2-3 miles	20-30 miles	20-2000 + miles	20-30 miles	Worldwide
Typical Use	Space limited and lower data rate applications	Computer networks	Long haul and networks	General communications; LOS (UHF)	Where cable laying not practical	Worldwide applications.

Table 1.1: General Comparison of Transmission Media [After Reference 1: p. 77].

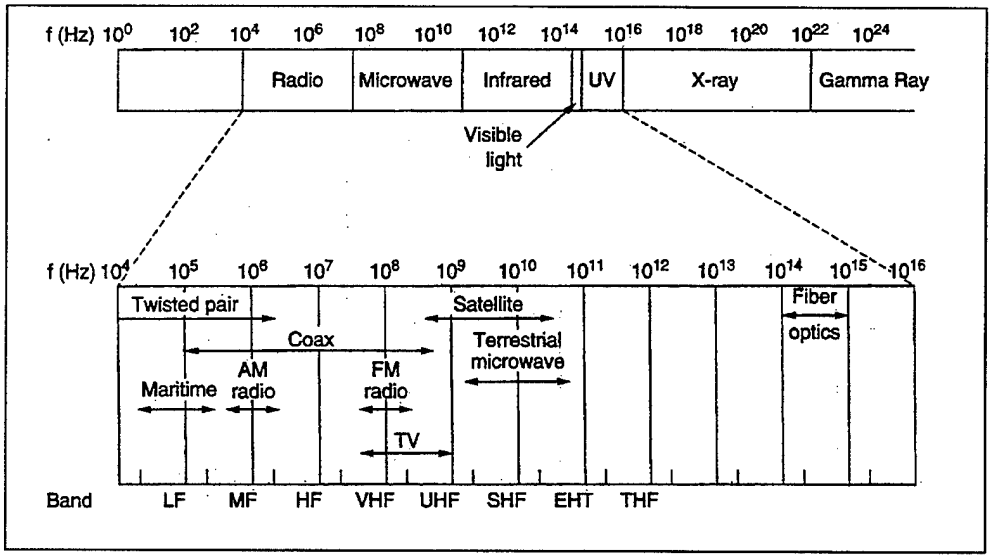


Figure 1.1: Electromagnetic Spectrum and Transmission Media [From Reference 2: p. 95].

Internal to the naval unit, physical connection media are the most beneficial means of transmitting data among the various communications and data processing systems.

Traditionally, copper media are used aboard ship. The use of this type of media onboard a modern naval combatant has certain undesirable consequences. Among them are (1) large, bulky cable runs (which may violate the ship's damage control integrity); (2) the added weight from these cable runs and their shielding; (3) difficulties in maintenance, troubleshooting, and system upgrades; and (4) interference due to electromagnetic interference (EMI). Crosstalk between wiring, electronic emissions which may be detected or intercepted, and electromagnetic compatibility (EMC) difficulties among the ship's electronic systems also pose problems. These adverse effects can be reduced or even eliminated with the use of optical fiber as the transmission medium. Optical fiber significantly reduces the size and weight required for cable runs while improving system maintainability and redundancy. System upgrades are easier and relatively less expensive. Virtually all problems with crosstalk, EMI, and electromagnetic compatibility may be reduced or eliminated due to the inherent physical properties of optical fiber. Data transmission is more secure than traditional electrical transmission, too. Table 1.2 summarizes the advantages of using fiber optics onboard surface ships.

Due to a combination of technological advancements, the requirements for precision munitions, high resolution battle damage assessment (BDA), and the unacceptability of significant civilian and friendly force losses, today's warfighter requires a significant amount of data relevant to the battle space in order to conduct the mission successfully and accurately. To meet these demands, user friendly C4I systems such as the Joint Maritime Command Information System (JMCIS) and the Global Command and Control System (GCCS) have been developed. However, the coupling of real-time data and digital imagery with the graphical nature of modern tactical data processing systems mandates a very large bandwidth and a high performance communications system. This is evident in Figures 1.2 and 1.3 which detail typical bandwidth requirements for the respective naval communications services and RF frequency bands [Reference 3: p.59]. With recent technological advancements, optoelectronics and optical fiber links can meet the demands of a large bandwidth, high-speed communications system. The large bandwidth illustrates

Technical Features	Benefits
Electromagnetic effects	• Not susceptible to EMI since it is a passive component • No crosstalk • No ground loops
Survivability	• Battle and fire damage reduced because of redundant paths • Not susceptible to EMP • Isolation of data from power source
Functional Requirements	• Occupies less space than other cables • Low weight • High data rate
Flexibility	• Long cable runs possible and few restrictions on cable routing • Supports high-speed LANs • Spare fiber will support system growth
Cost	• Reduced cost for installation and maintenance
Components	• Simplified technology reduces required components

Table 1.2: Advantages of Using Fiber Optics in Surface Ships [After Reference 3: p. 432].

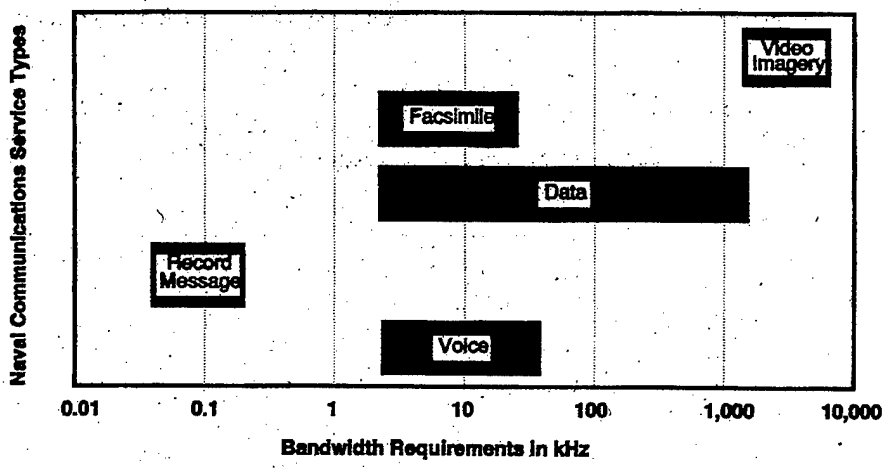


Figure 1.2: Bandwidth Requirements for Naval Communications Services [From Reference 3].

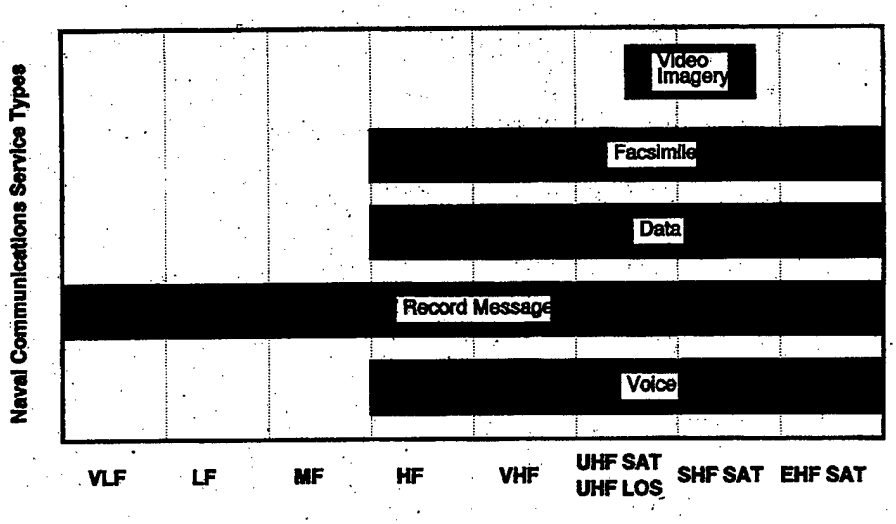


Figure 1.3: Use of RF Bands by Naval Communications Service Types [From Reference 3].

another advantage of optical fiber over the coaxial cable traditionally used in naval communications systems. Signal loss in coaxial cable is frequency dependent. As signal frequency increases from the tens of megahertz to the gigahertz range, signal loss grows exponentially (see Figure 1.4). For point-to-point links over several meters (common onboard naval vessels), this frequency dependent signal loss is not trivial. Optical fiber eliminates the frequency dependent signal loss problem.

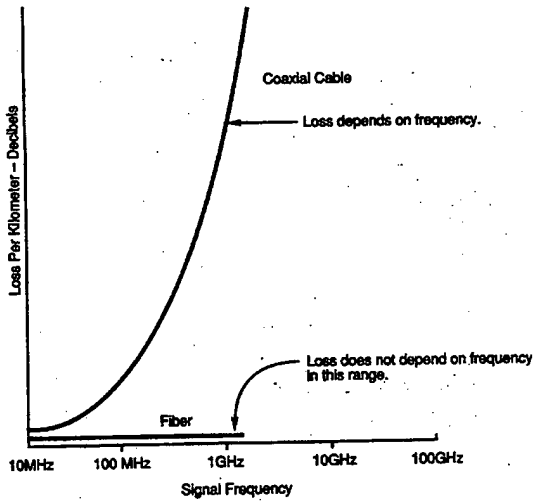


Figure 1.4: Coaxial Cable Signal Loss Versus Optical Fiber Signal Loss [From Reference 4].

C. DESIGN REQUIREMENTS

To be an effective and effective communications link for the modern warfighter, a data link must be a cost-effective system meeting budgetary constraints, must have an effective RF antenna system, must meet or exceed EMC requirements, and must be able to transmit and receive a large volume of data at a very high rate. The aforementioned requirements are the design goals for the data link developed in this thesis.

To meet the financial constraints, COTS components were selected to reduce the expense of the data link. To meet EMC, bandwidth, and high speed requirements, a data link consisting of optical fiber, semiconductor lasers and photodetectors was designed. Additionally, the Transistor-Transistor Logic (TTL) family, the Emitter Coupled Logic (ECL) family, and other linear integrated circuits were used in this design. An overview of the data link is described in the next section.

Additional design requirements were imposed on the electro-optical data link design to support ongoing research at the Naval Postgraduate School into a high-resolution digital antenna system. To enable interoperability with the digital antenna system's electro-optic analog-to-digital converter (ADC), the data link at a minimum must support 14-bit data words at 5 Mword/sec (millions of data words per second). Further, the two ADC architectures, a symmetric number system folding circuit and an electro-optic sigma-delta design, being developed for the high-resolution digital antenna system potentially may provide up to 24-bit data words at a 100 Mword/sec (or greater) data rate. This would provide a very high resolution antenna system capable of operating in the very high frequency (VHF) range. The components selected for the data link support up to 21-bit data words at 50 Mword/sec (or up to 17-bit data words at 60 Mword/sec). While the current components may not support the predicted performance of the high-resolution digital antenna system, they provide sufficient capacity and speed for the digital antenna system in the near future. By the time the digital antenna system is performing near the upper design limits, suitable commercial components similar to those used in this data link should be

readily available at an economical price. Lessons learned during this research may be applied to subsequent data link design for the high-resolution digital antenna system. [References 5, 6, and 7]

D. OVERVIEW OF THE MULTI-CHANNEL HIGH-SPEED DATA LINK

The high-speed data link in question is part of continuing research at the Naval Postgraduate School into a high-resolution digital antenna system. The digital antenna system (see Figure 1.5) is comprised of a receiving RF antenna , an electro-optic analog-to-digital converter (ADC), a high-speed optoelectronic transmitter, a fiber optic link, a high-speed optoelectronic receiver, and the necessary signal processing equipment.

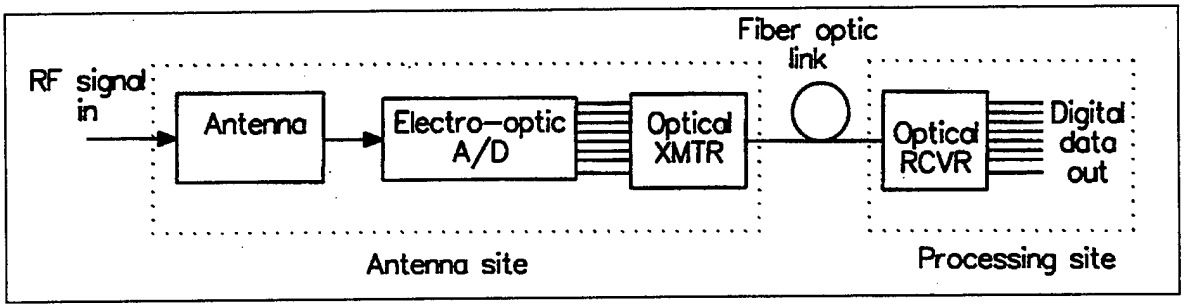
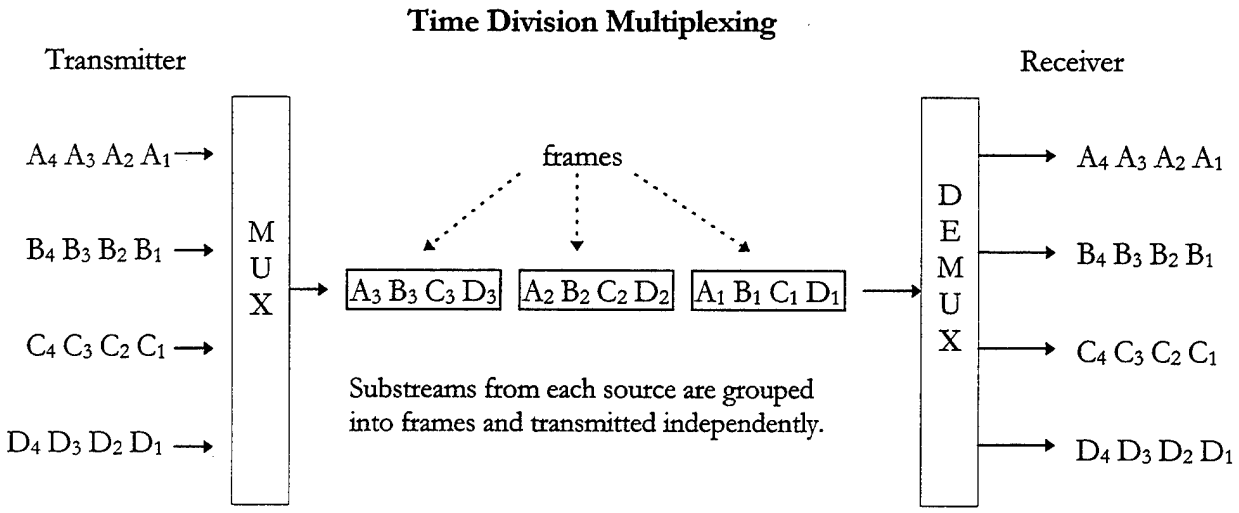


Figure 1.5: Overview of the High-Resolution Digital Antenna System [From Reference 5].

The system uses the electro-optic ADC to convert the received RF signal into a 14-bit binary word which is input into the optoelectronic transmitter. The transmitter converts the 14-bit binary words into a serialized stream of binary data and uses a laser to transmit the serialized binary data stream through the optical fiber. This method is known as time division multiplexing (TDM) and is illustrated in Figure 1.6. To recover the transmitted data, the optoelectronic receiver detects the binary data stream sent through the optical fiber and converts it into 14-bit binary words which are used by the associated signal processing system. Due to the high speed of the transmitter-receiver pair, the data stream appears to the user to be a *virtual ribbon cable* of fourteen channels. The signal processing equipment

can then process the received data words and route the information to the proper computing systems (such as a tactical data processor).



Signal sources: A_i, B_i, C_i, and D_i represent bit streams.

Figure 1.6: Time Division Multiplexing [After Reference 1: p. 156].

In this chapter, an overview of the multi-channel, high-speed, fiber-optic digital data link was described. Chapter II details the design and implementation of the data link's transmitter subsystem.

II. TRANSMITTER SYSTEM DESIGN

A. TRANSMITTER SYSTEM CONCEPTS

The general concept of the transmitter system in the high-speed, multi-channel data link can be described by its three basic functions: (1) convert the received analog signal into binary words, (2) convert the binary words into a serial stream of binary bits, and (3) transmit the bit stream to the receiver system. A high-speed analog-digital converter (ADC) was used to convert the received RF analog signal into 14-bit binary words. Depending on the speed and accuracy of the ADC, the 14-bit words can be in the tens of millions of words/second (Mwords/sec) range. These tens of 14-bit Mwords/sec are converted by a high-speed parallel-serial converter. In other words, each 14-bit parallel word is converted into a sequence of 14 bits. The serial data rate is 14 times the parallel word/sec rate (in Mbits/sec). Neglecting frame overhead, the serial data stream is then transmitted through a high-speed optoelectronic transmitter and into an optical fiber link. Here the serial data rate can exceed 1 Gigabit/sec. A functional block diagram of the transmitter system is shown in Figure 2.1.

For the high-speed, multi-channel, optoelectronic digital data link, a function generator was used to generate a time-varying analog signal to simulate the received RF signal. The analog signal is sent through a Datel ADS-944 14-bit, 5 MHz sampling A/D converter. For this thesis, the Datel electronic ADC is used in lieu of the high-speed optoelectronic ADC under development at NPS. The ADS-944 provides 14-channels of data at a moderately high speed (5 MHz) giving a data rate of 5 Mwords/sec. Although this data rate is 10-12 times slower than the maximum data rate of the link (depending on word size[1]), it provides a sufficiently high data rate to test the data link for correct operation. The output of the ADC is routed to the BCP 15T G-Link fiber optic transmitter. This module uses a Hewlett-Packard HDMP-101X series G-Link chip set which has the ability to convert

16-17 or 20-21 bit words into a high-speed serial bit stream appearing as a *virtual ribbon cable* to the user. The HDMP chip set may be used with coaxial cable or optical fiber. In this design, the chip set drives a 1310 nm semiconductor laser which converts the electrical bit stream into an optical bit stream transmitted through optical fiber. The fiber link may be anywhere from 1 m to 1 km (for multi-mode fiber) or 1 m to 10 km (for single-mode fiber). [Reference 8]

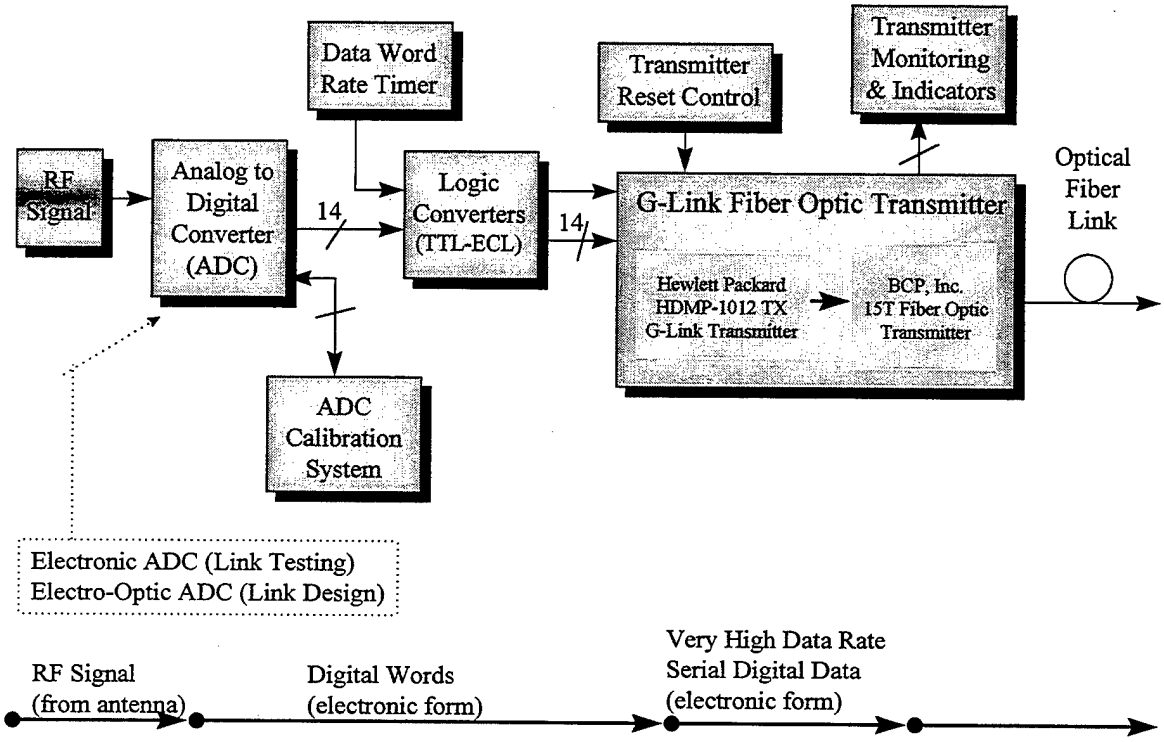


Figure 2.1: Functional Diagram of the Electro-Optic Transmitter System.

The BCP G-Link set may be procured with either a 1310 nm or 1550 nm InGaAsP-based semiconductor laser. The 1310 nm variant was selected primarily due to the lower cost versus the 1550 nm variant. (The 1310 nm point is the zero dispersion point of silica fiber. The wavelength of lowest attenuation in silica fibers occurs at 1550 nm.) On a shipboard scale fiber link (hundreds of meters), the lower cost laser should provide similar performance to the more expensive variant. Figure 2.2 shows the relationship between the

[1] The BCP 15T/R G-Link fiber optic modules used in this data link have the ability to transmit/receive 16 or 17 bit words at 60 Mwords/sec and 20 or 21 bit words at 50 Mwords/sec.

1310 nm, 1550 nm, and LED (850 nm) frequency bands versus signal attenuation (in dB/km). [Reference 9] The lasers used in the 15T have a spectral width of approximately 4 nm and a peak optical output power of –9 dBm. The transmitter laser is connected to a 9/125 μm single-mode fiber pigtail. Semiconductor lasers vice LEDs are the preferred choice in this high-data-rate system due to their better attenuation, dispersion, and optical power performance as seen in Figures 2.2 and 2.3. (For a more comprehensive introduction to semiconductor lasers, LEDs, fiber optics, and photodetectors refer to References 9, 10, and 11.)

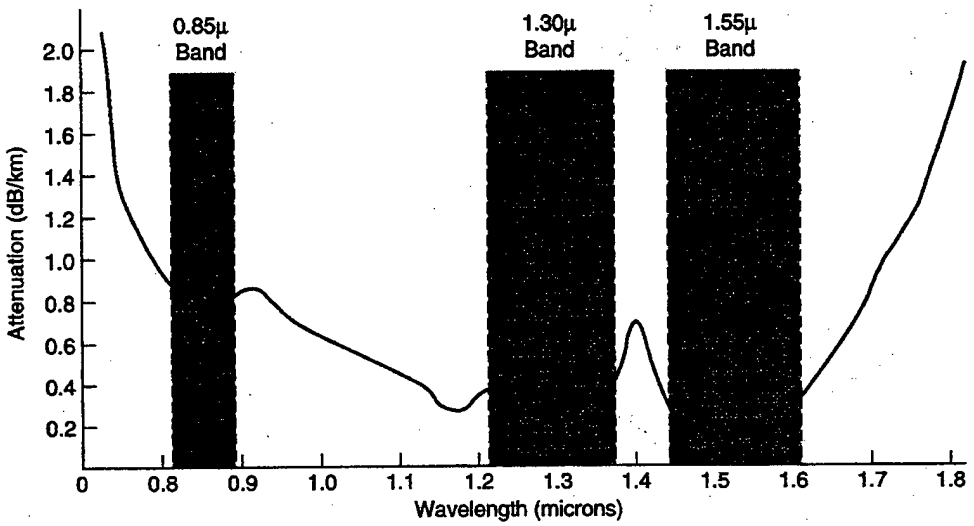


Figure 2.2: Semiconductor LED and Laser Bands in Silica Fiber [From Reference 2: p. 89].

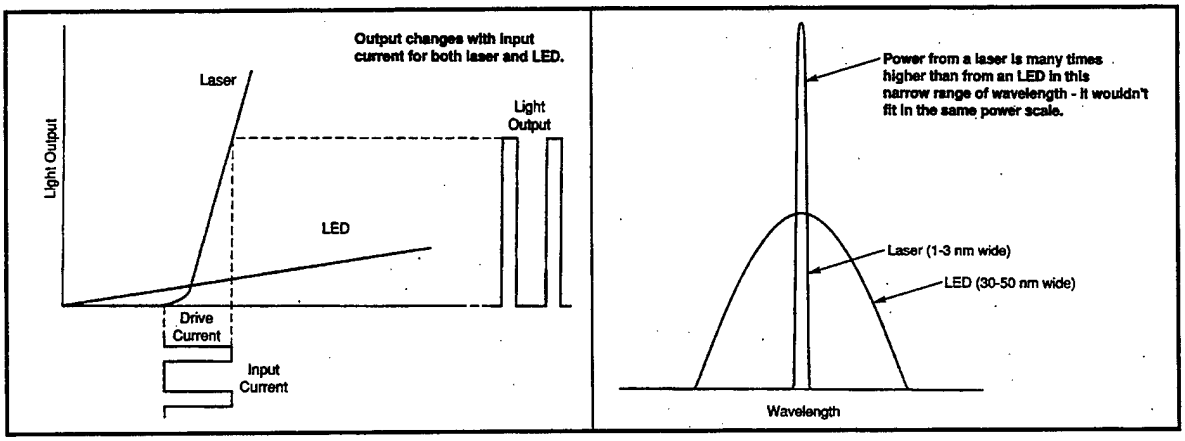


Figure 2.3: Superior Performance of Semiconductor Lasers Versus LEDs [From Reference 4].

B. OVERVIEW OF TRANSMITTER SYSTEM COMPONENTS

The electro-optic transmitter system is a key component of the digital antenna system. The transmitter system interfaces with the digital antenna's electro-optic ADC and routes the digital antenna data through the G-Link fiber optic transmitter system to the receiver system. The flow of data in the transmitter system is readily seen in Figure 2.1 above. Physically, the prototype system consists of the electronic Datel ADC evaluation board, an ADC control board, and the fiber optic transmitter control board including the fiber optic transmitter module. The ADC and ADC control board use TTL-compatible interfaces. The TX board has a TTL-compatible input interface and an ECL-compatible output interface. The following sections of this chapter describes each of the transmitter components and how they were integrated into the transmitter system design.

1. Datel ADS-944 A/D Converter

The A/D converter used to test and demonstrate the high-speed data link is the Datel ADS-944 14-bit, 5 MHz Sampling A/D Converter. The ADC features 14 bit resolution, both an external and on-board control of the A/D conversion process, and low power consumption. It also operates in military temperature ranges. Higher frequency sampling A/D converters are available in the industry, but as the resolution and frequency increases so does the cost [Reference 12]. The features and functions provided by the ADS-944 were sufficient for initial testing and evaluation of the data link. The ADC can achieve a Total Harmonic Distortion (THD) range of –77 dB and has a Signal-Noise Ratio (SNR) of 76 dB. All digital inputs and outputs are TTL compatible. Flash A/D conversion along with a Digital-Analog Converter and digital correction logic allow the ADC to perform accurately with a high resolution [Reference 13]. A functional block diagram of the ADC is shown in Figure 2.4. Data sheets are included in Appendix A.

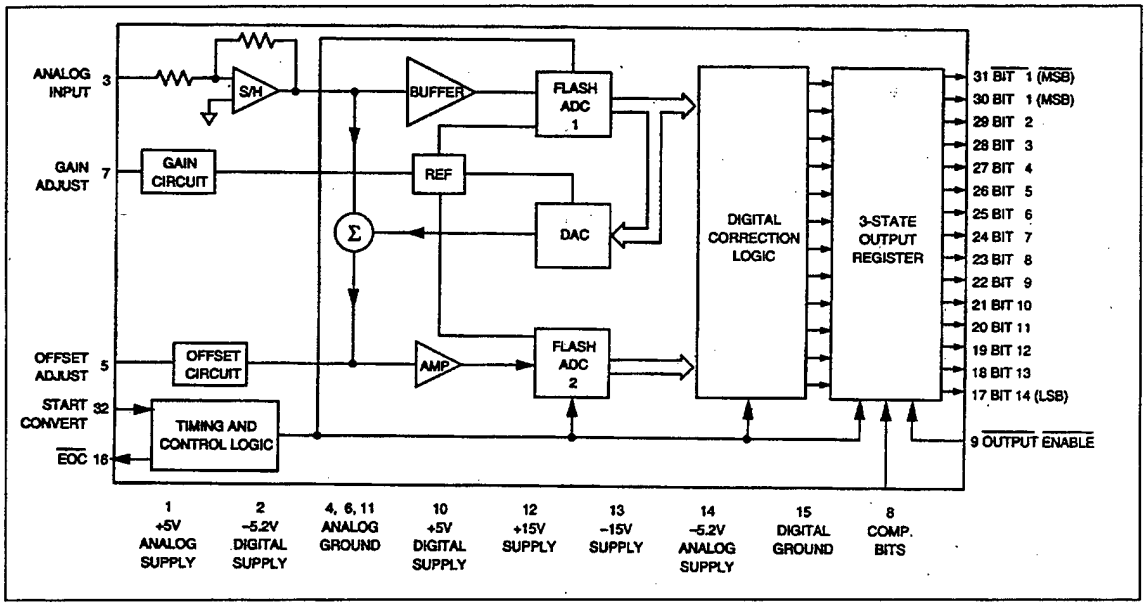


Figure 2.4: Functional Diagram of Datel A/D Converter ADS-944 [From Reference 13: p. 1-143].

2. BCP 15T Gigabit Fiber Optic Digital Transmitter Module

At the heart of the transmitter system is the BCP 15T TX module. The module consists of the transmitter portion of the Hewlett-Packard gigabit rate transmit/receive chip set and the Broadband Communications Products Model 15T high-speed parallel-to-serial fiber optic transmitter. The G-Link module has applications in backplane, video, image acquisition, and high-performance point-point data links [Reference 14]. The HP G-Link chip set consists of an HDMP-1012 transmitter chip and an HDMP-1014 receiver chip. The G-Link chip set is based on Hewlett-Packard's 20-bit/24-bit encoding scheme for gigabit rate data acquisition. The scheme was eventually adopted in 1992 as an ANSI standard for the Serial-HIPPI (High-Performance Parallel Interface) signaling protocol [Reference 15]. (The Serial-HIPPI protocol is a derivative of the high-performance HIPPI protocol developed for supercomputing at the Los Alamos National Laboratory [Reference 2: pp. 325-326]. Further information regarding HP's Serial-HIPPI standard is found in references 15, 16, and 17.)

The HDMP-1012 transmitter when used in conjunction with the HDMP-1014 receiver may be used in either a full-duplex or a simplex configuration. The

transmit/receive modules may be used with coaxial cable for short distance links (20-30 m) or with optical fiber for longer distance links (up to 10 km with single mode fiber). The key benefit of these modules is they have the ability to transmit/receive parallel words at a very high serial data rate making the data link appear to be a virtual ribbon cable to the user.

The full-duplex configuration allows two TX/RX module pairs to simultaneously transmit and receive data at a high rate. This bi-directional link is ideal for transmit-receive communication systems. (Refer to Figure 2.5 for a typical full-duplex configuration.) The two TX/RX module pairs are synchronized through the use of the HDMP-1014 RX state machine. This configuration also provides the link designer with three loopback options for fault isolation and testing of the link. Local loopback allows the G-Link chip set to be tested independent of the optical transmitter and receiver. Remote loopback is used to test the link connection between two pairs of 15T/R G-Link modules. Lastly, optical loopback is used to test the correct operation of the optical transmitter and the G-Link chip set [Reference 8]. For a graphical diagram of the different loopback configurations available with the G-Link chip set in Full-Duplex Configuration, refer to the BCP Data Notebook [Reference 8].

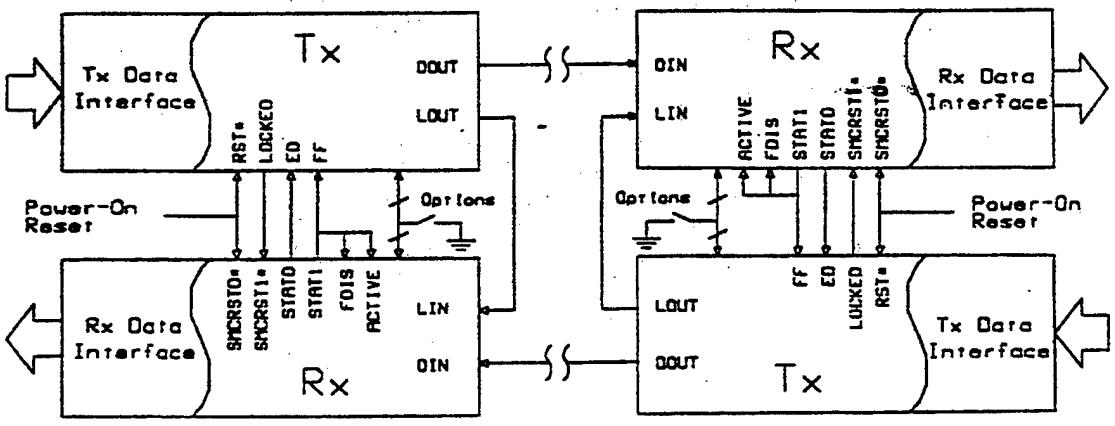


Figure 2.5: G-Link Full-Duplex Configuration [From Reference 14: p. 33].

The high-resolution digital antenna systems requires a unidirectional (or simplex) data link. Therefore, one of the three G-Link simplex configurations must be selected for

the design in this thesis. The simplex configurations are shown in Figures 2.6 through 2.8 below. Simplex Method I (Figure 2.6) is a simplex configuration using a low-speed return path. The low speed return lines are used to synchronize the link between the TX and RX. A disadvantage of this method for use in the digital antenna system is that additional cable runs for the low-speed control wiring would have to be placed between the TX and RX in addition to the connecting optical fiber. This will reduce the weight and space savings of just using an optical fiber connection between the TX and RX. Further, inherent delays in the low speed return lines cause a performance hit on the links maximum data rate. Simplex Method II (Figure 2.7) eliminates the low speed lines and uses a periodic sync pulse which disables data transmission from the TX for a short period of time. During this period, fill frames are sent through the optical link allowing the RX to re-synchronize itself with the TX. Although this method is an improvement over Simplex Method I, the link is unavailable during the sync pulse periods and the control logic complexity is increased. The optimal simplex configuration for the high-resolution digital antenna system is Simplex Method III (Figure 2.8). This configuration requires only the optical fiber connection and allows the link to potentially operate at its maximum data rate. Method III uses two high-speed oscillators (one local to the TX and one local to the RX) to enable link synchronization. The TX local oscillator is used to multiply its internal clock to the required serial data rate. The RX uses its local oscillator as a reference oscillator that when used with the RX Phase-Lock Loop (PLL) enables the RX to synchronize with the TX. The time required for the RX to lock onto the TX data stream is proportional to the difference between the local TX and local RX oscillators. So long as there is at least a slight difference between the oscillator frequencies, this method will be effective. Typical crystal oscillators rated for the same oscillator frequency vary from each other by a typical factor of 0.001 to 0.00001. So long as the individual oscillator frequency matching falls within this range this method will work correctly. Should the frequency difference exceed the 0.001 factor an excessive time will be spent acquiring and reacquiring lock onto the transmitter's

optical data stream. [Reference 14: pp. 34-35] Simplex Method III was the method used in the high-speed, multi-channel data link design.

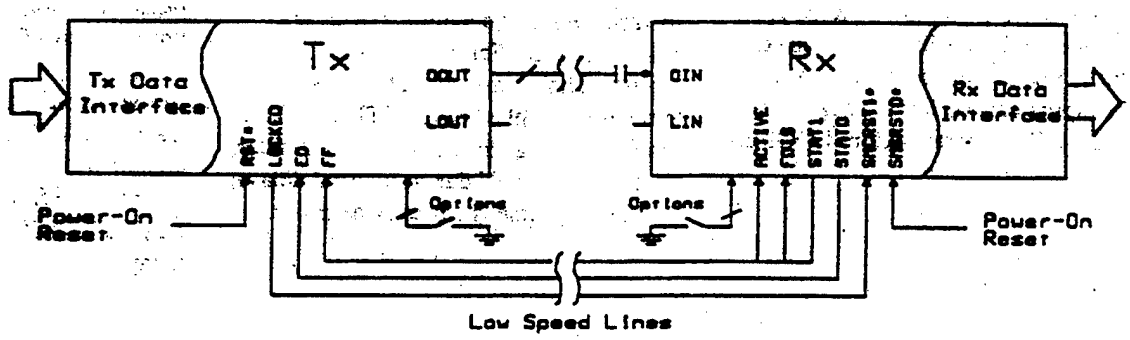


Figure 2.6: G-Link Simplex I Configuration [From Reference 14: p. 34].

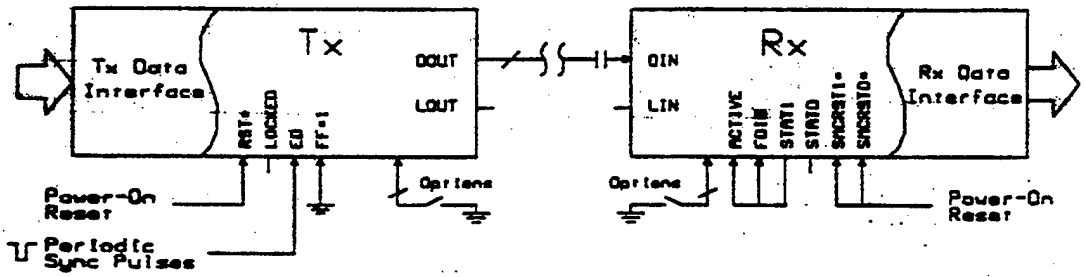


Figure 2.7: G-Link Simplex II Configuration [From Reference 14: p. 34].

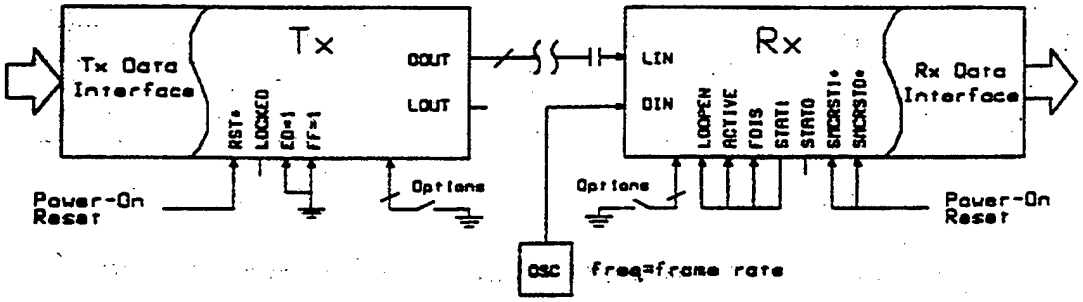


Figure 2.8: G-Link Simplex III Configuration [From Reference 14: p. 34].

The HDMP-1012 TX is designed to perform four functions: (1) receive a 16-bit or 20-bit parallel word input, (2) multiply the reference parallel word rate to achieve a high-speed serial clock, (3) encode data and control word frames, and (4) perform parallel to serial multiplexing. Figure 2.9 is a functional block diagram of the HDMP-1012 TX module. For the Simplex III configuration, the TX operates (1) by latching a 16 or 20-bit

word available on the data (D0..D19) lines at the rising edge of STRBOUT, (2) by multiplying the reference clock input (STRBIN) to achieve the serial data rate, (3) by encoding the 20 or 24-bit frame depending upon control inputs such as CAV*, DAV*, FLAG, FLAGSEL, M20SEL, and (4) by clocking the encoded serial frame to the 15T high speed parallel-serial fiber optic transmitter. If FLAGSEL is enabled, an additional data bit will be latched on the FLAG input line. To maintain a DC balance on the transmission lines, sequential frames alternate between complemented and uncomplemented formats.

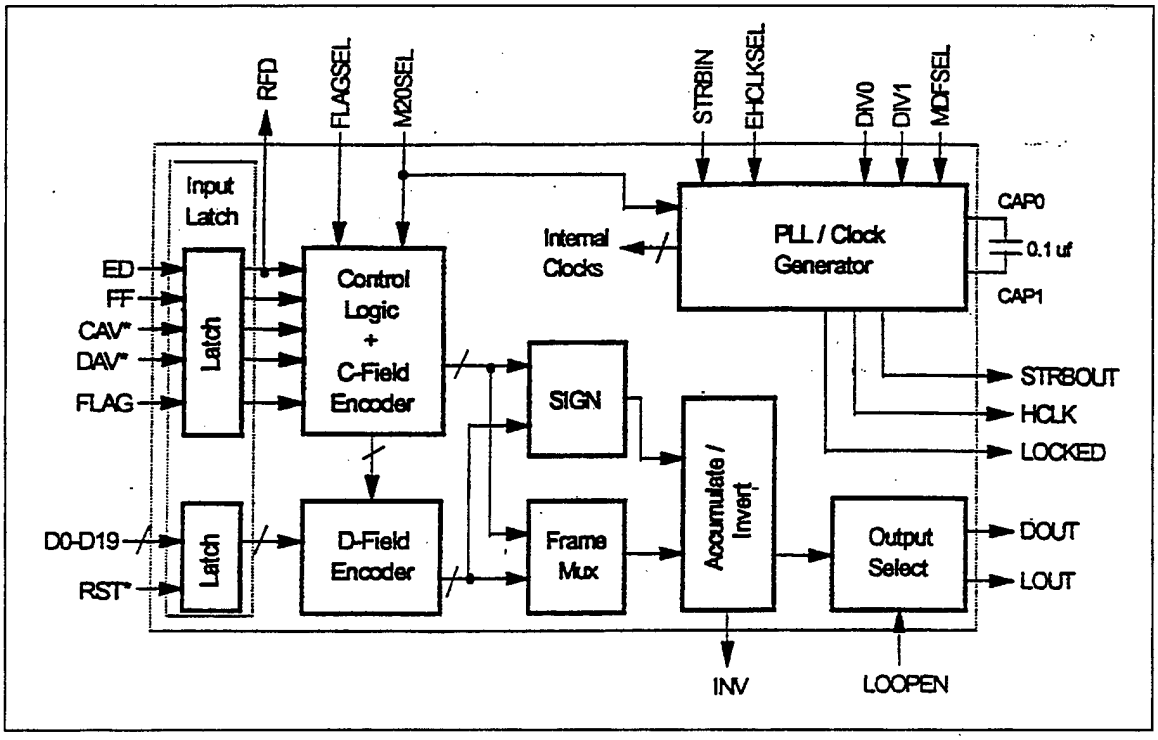
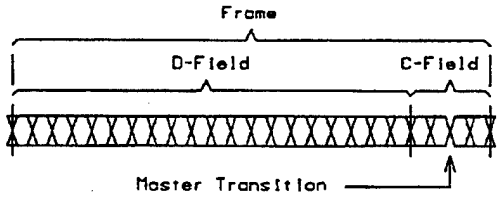


Figure 2.9: Functional Diagram of HDMP-1012 TX [From Reference 14: p. 6].

The CAV* (Control Word Available) and DAV* (Data Word Available) control lines tell the TX whether the word on the data lines is a control word or data word. This feature allows the data link to differentiate between data and control information which is beneficial for using data link protocols such as Internet Protocol (IP) variants or Serial-HIPPI . The FLAGSEL control line determines whether the FLAG bit is used as an additional data line (which would provide 17 or 21 bit words) or if it is used as an additional

error detection bit. The FLAG bit is determined by polarity of the master transition in the information frame (see Figure 2.10). When FLAGSEL is not enabled, the FLAG bit differentiates between even and odd frames and provides an extra bit for error detection.



C-Field	D-Field	Flag Bit
1 1 0 1	True	0
0 0 1 0	Inverted	0
1 0 1 1	True	1
0 1 0 0	Inverted	1

Figure 2.10: G-Link Frame Format [From Reference 17: p. 227].

The aforementioned control lines, along with M20SEL (16 or 20-bit mode select), are used by the control logic, the C-Field encoder, and the D-Field encoder to determine proper word encoding. The C-Field describes the frame type (data, control word, fill frame) and is used for error detection. The D-field is nothing more than the data or control word information bits. The frame multiplexer concatenates the C-Field and D-Field information to form a proper frame for transmission. The accumulate/invert module is used to alternate sending complemented and uncomplemented frames which maintains the DC balance through the link's transmission lines. Output select determines whether the serial output is sent via coaxial cable (LOUT) or optical fiber (DOUT). In the Simplex III configuration, output is sent via the DOUT line. The 15T Fiber Optic Transmitter is used to convert the electrical data into light waves sent through the optical fiber with a 1310 nm wavelength semiconductor laser diode[2].

[2] A 1550 nm wavelength semiconductor laser is also available from BCP.

C. TRANSMITTER DESIGN DETAILS

To implement the Simplex III configuration, several prototype boards were designed and built. An ADC control board was designed to provide necessary power supply routing and A/D conversion control. Fourteen bit data words were generated using the ADS-944 Evaluation Board and a function generator which generated the analog input signal. A TX control board was also built which consisted of a bank of LEDs to be used in calibration of the ADC, TTL-ECL converters, the 15T fiber optic transmitter module, and assorted control logic. The RX control board is described in Chapter III.

1. ADC Control Board

The A/D conversion control board has two primary functions: (1) to route power and ground supplies for proper ADS-944 operation and (2) to create a customizable START_CONVERT pulse. The power supplies required for the ADS-944 ADC chip consist of both analog (floating) and digital (chassis) voltage references. The control board was designed to route all analog and digital reference voltages as required by the ADS-944 schematics. Improper connection of the proper power supplies may cause an excessive current through the ADC. If not corrected, this may cause severe overheating of the ADC. The routing of supplies and custom START_CONVERT pulse generation is shown in the A/D Converter Control Board diagram (Figure 2.11).

The alternate START_CONVERT generation requires a TTL level crystal oscillator, a 74163 Binary Counter, and a 74121 Monostable (Non-retriggerable) Vibrator or *One Shot*. If the oscillator clock signal exceeds the ADC's sampling range (greater than 6.6 MHz), the binary counter is setup as a divide counter. In this configuration, the divide counter will divide the clock signal into the sampling range. The *One Shot* is used to generate either a 40-80 ns or 130-160 ns wide start convert pulse. The leading edge of the START_CONVERT pulse initiates the A/D conversion process. The pulse must be within one of the two pulse width ranges to prevent the ADC from re-triggering the conversion process. The benefit of using a customizable START_CONVERT pulse is that applications

requiring lower than a 5 MHz sampling rate may be performed. In the data link design, most A/D conversion was conducted using the 5 MHz sampling rate with the oscillator on-board the ADS-944 Evaluation Board.

The custom START_CONVERT generation was used to verify the correct operation of the ADS-944 ADC. The conversion rate can be modified by a combination of changing the crystal oscillator frequency (through swapping with a different frequency crystal) and selecting the appropriate divide output of the 74163. The 74163 has four divide outputs (QA, QB, QC, QD) which represent dividing the output by 2, 4, 8, or 16, respectively. Pulse width timing for the conversion process is controlled by the 74121 one shot. The pulse width may be varied through the use of Equation 2.1:

$$t_{w(out)} = C_{ext} \cdot R_t \cdot \ln 2 \tag{2.1}$$

where C_{ext} is the external capacitance, R_t is the value of the timing resistor, and t_w is the timing pulse width. Refer to Appendix A for more detailed specifications of these logic devices.

Figure 2.12 shows a comparison between the custom and internal START_CONVERT signals. An attempt was made to produce a cleaner custom conversion signal by using a voltage comparator to drive the signal between the rail voltages of 0 Vdc and +5 Vdc. TTL-compatible high-speed linear voltage comparators such as the LM311 and LM710 do not provide sufficient switching speed to produce the correct timing signal. Since the ADC triggers on the rising edge of the conversion signal and works correctly as designed, the decision was made to not use a more expensive, very high-speed TTL-compatible voltage comparator to provide a cleaner TTL timing signal.

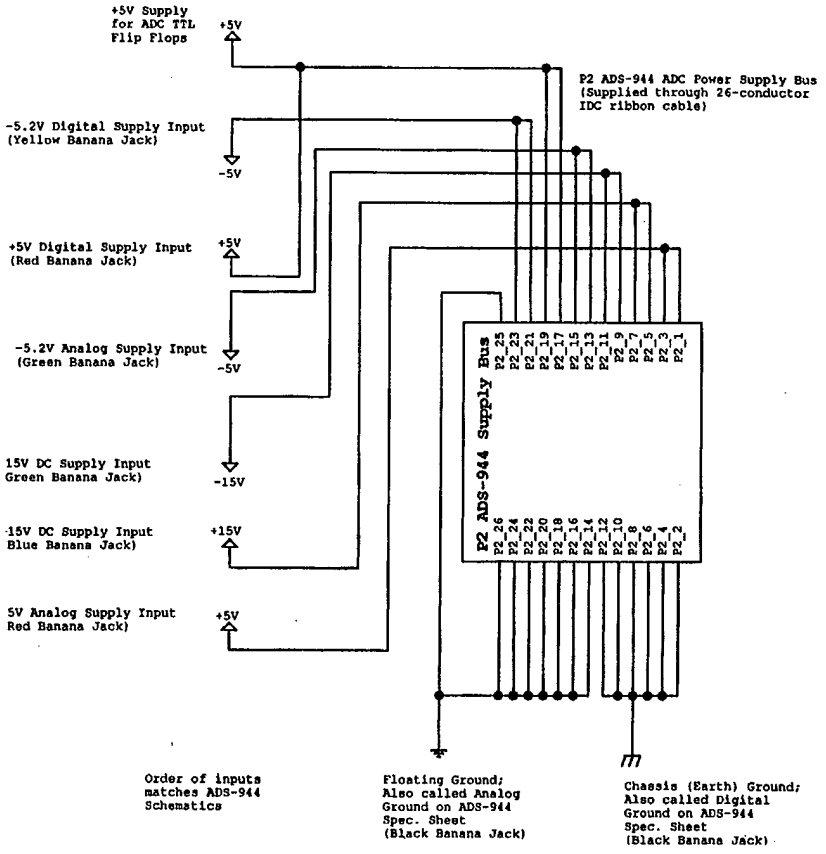


Figure 2.11: A/D Converter Control Board Schematic.

ADS-944 Analog to Digital Converter Control Board

Start Convert Generation
5 MHz Clock with 60 ns pulse width

ADS-944 requires start convert pulse width between 40-80 ns or 130-160 ns to ensure proper operation.

Minimum sampling rate: 5 MHz

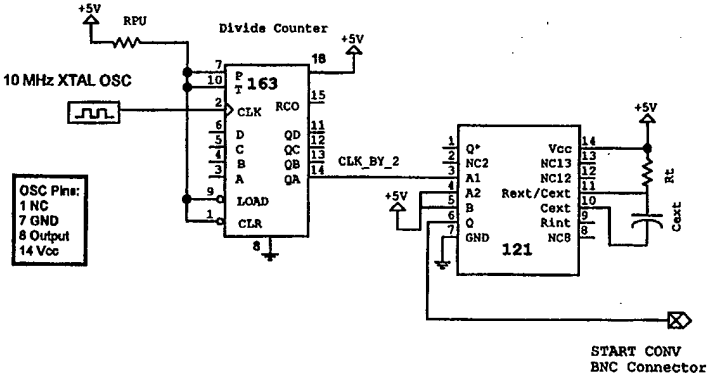
Max. sampling rate: 6.6 MHz

Pulse width calculation:

Fix Ct=0.001uF

tw(out) = Cext Rt ln2

For tw(out) = 80ns
Rt = 80ns/(0.001uF * ln2)
= 115 Ohms



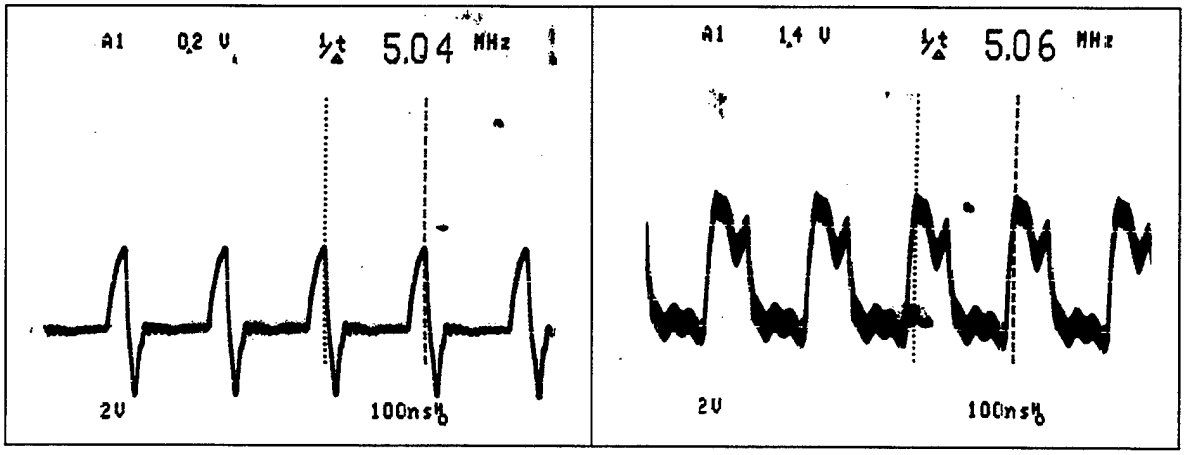


Figure 2.12: A/D Converter Custom Versus Internal START_CONVERT Signals.

2. ADS-944 Evaluation Board

The ADS-944 Evaluation board (Figure 2.13) was used to generate 14-bit words from the analog signal input generated by the function generator. Power and ground supplies were routed from the A/D Converter Control Board described above. Integrated circuit pin-outs, connector routing information, and data sheets are located in the ADS-944 section of Appendix A. The ADC required the analog input signal to be in the +/– 1.25 V range. Any input voltage above this range would translate to the +1.25 V bit encoding. Likewise, any input voltage below would translate to the –1.25 V bit encoding. The ADC calibration procedure and timing diagrams are also found in Appendix A. The TTL level data outputs are routed from the P1 bus connector to the TX Control Board.

Following verification of correct ADC operation with the custom START_CONVERT signal, JPR 3 was set to enable the internal conversion frequency to test the data link operation. JPR 1 was set to enable offset binary mode operation. Note the end of conversion (EOC*) signal can be used to determine when the ADC outputs valid data (Figure 2.14).

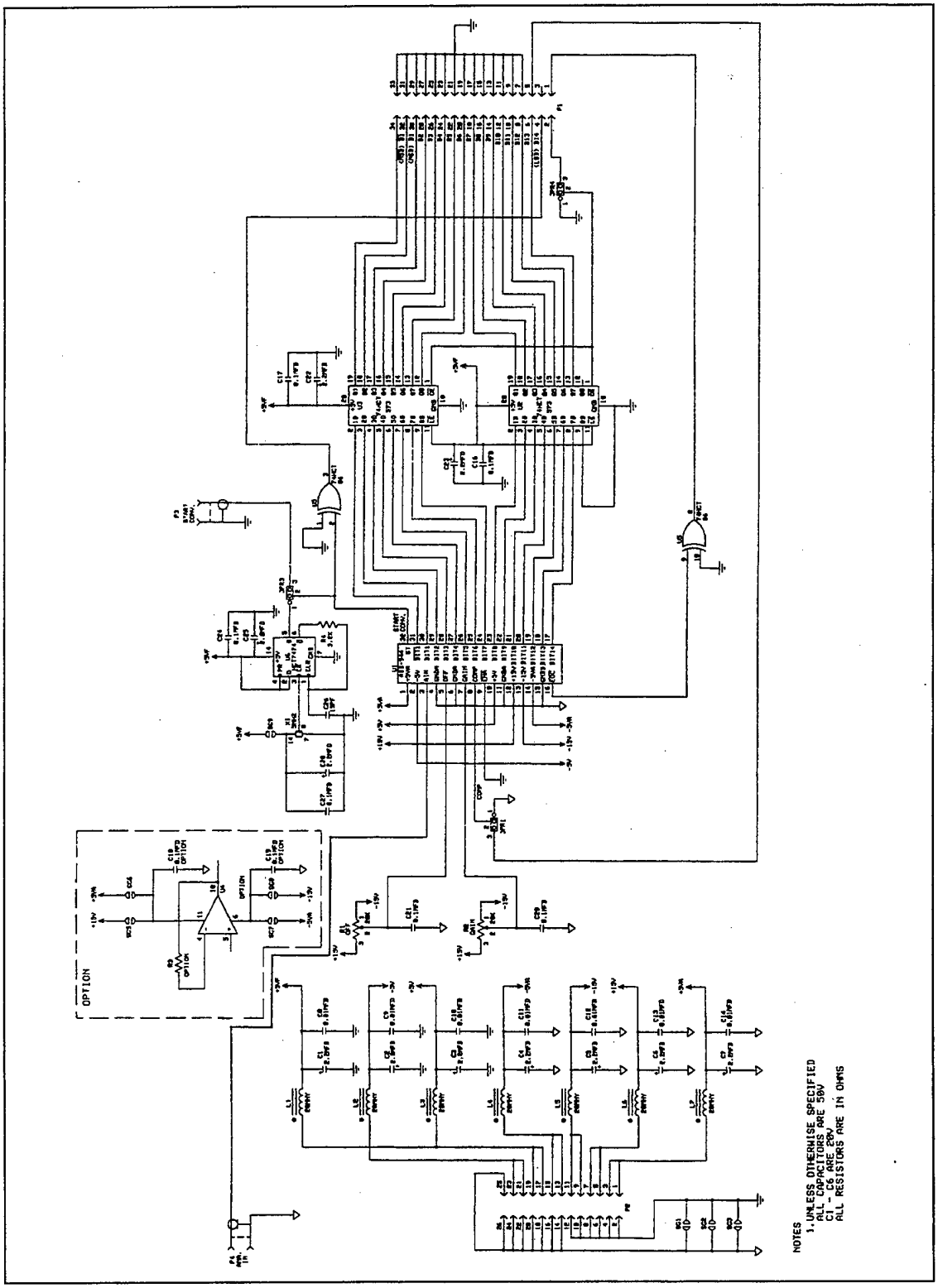


Figure 2.13: ADS-944 ADC Evaluation Board Schematic [From Reference 13: p. 1-148].

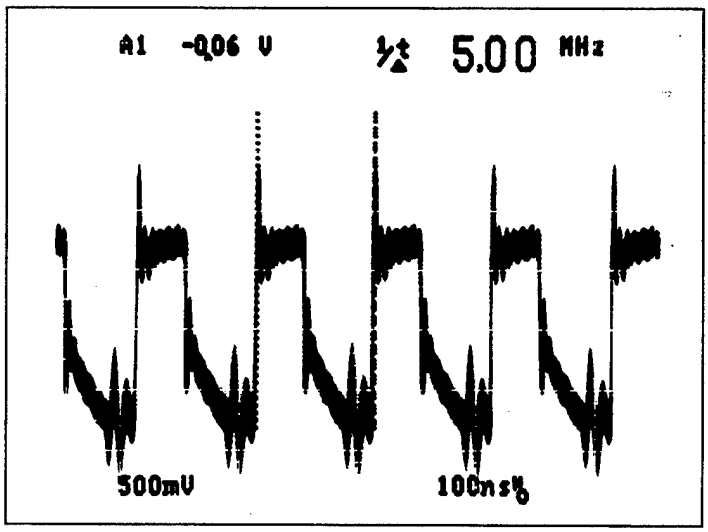


Figure 2.14: EOC* Signal Generated by the ADC.

ADC calibration is conducted following the procedure listed in the Datel data book [Reference 13: p. 1-146]. Note the procedure calls to apply a voltage of +76.3 mV for the offset adjust procedure and a voltage of +1.249771 V for the gain adjust procedure. Due to the precision of the power supply equipment, these voltages cannot be attained exactly. Therefore, some inaccuracies appear in the lower order bits when compared to the output coding values. Typically the observed effect is that the least significant bits stay at the logic one level.

3. TX Control Board

The TX Control Board (Figure 2.15) receives the 14-bit data words from the ADC along with the OE* (output enable), COMP (complement), and START_CONVERT signals. A bank of LEDs on the TX Control Board was used in the ADC calibration procedures mentioned in Section II.C.2. In the calibration procedures, the LEDs will reflect the correct coding values when a fixed voltage between +/– 1.25 V is applied to the ADC's analog input.

The 14-bit data words are routed through MECL MC10124 TTL-MECL converters which translate the TTL data into ECL compatible logic levels. The TTL data lines coming from the ADC P1 bus are labeled B1..B14 with B1 being the most significant bit. Note that

the MC10124 converters are different from most ECL logic circuits in that they require V_{CC} = +5.0 Vdc vice digital ground. Also, the MC10124 requires +5.0 Vdc be applied to each of the common strobe (Com_Strb) inputs for logic conversion to take place. If digital ground is applied to Com_Strb, the converters will invert the data signals. The 14 ECL level data lines (labeled D0..D13 in the schematic) are connected to the 15T module (each with a pull-down resistor of 100 Ω to V_{TT}). The remaining 6 data lines and the FLAG input line on the 15T module are left as *no connects* which fixes them as ECL level logic zeros (due to internal pull-down resistors within the 15T module). Data line D0 is the most significant bit of the data word. Power and ground connections on the 15T module are as expected. Decoupling capacitors of 0.01 μF to ground were used on each V_{EE} connection.

The 15T/R modules and the HDMP-101X chip set comply to Motorola 100K family logic. The electronic particulars of emitter-coupled logic families are discussed in *Appendix B: Survey of Data Link Digital Design Considerations* and in References 18, 19, and 20. Most other ECL logic used for control logic on the prototype board designs complies to the Motorola MECL 10K logic family specifications. Generally, V_{EE} refers to the most negative power supply voltage (usually –5.2Vdc). V_{CC} is the most positive power supply voltage (usually digital ground). V_{CC} is typically +5.0 Vdc on TTL logic and ECL logic converters.

The remaining control signals were set to enable the Simplex III configuration (in accordance with References 8 and 14). A module reset switch is connected to the RST* pin of the fiber optic transmitter. The reset signal must be asserted for at least five parallel-rate clock cycles (approximately 500 ns in the 10 MHz implementation). A momentary push-switch was used in the prototype implementation for transmitter reset. The *normally open* position was tied to digital ground while the *normally closed* position was connected through a pull-down resistor to V_{TT}. The TX Locked and STRBOUT signals are used to indicate status of the TX module. Input data is latched on the rising edge of STRBOUT.

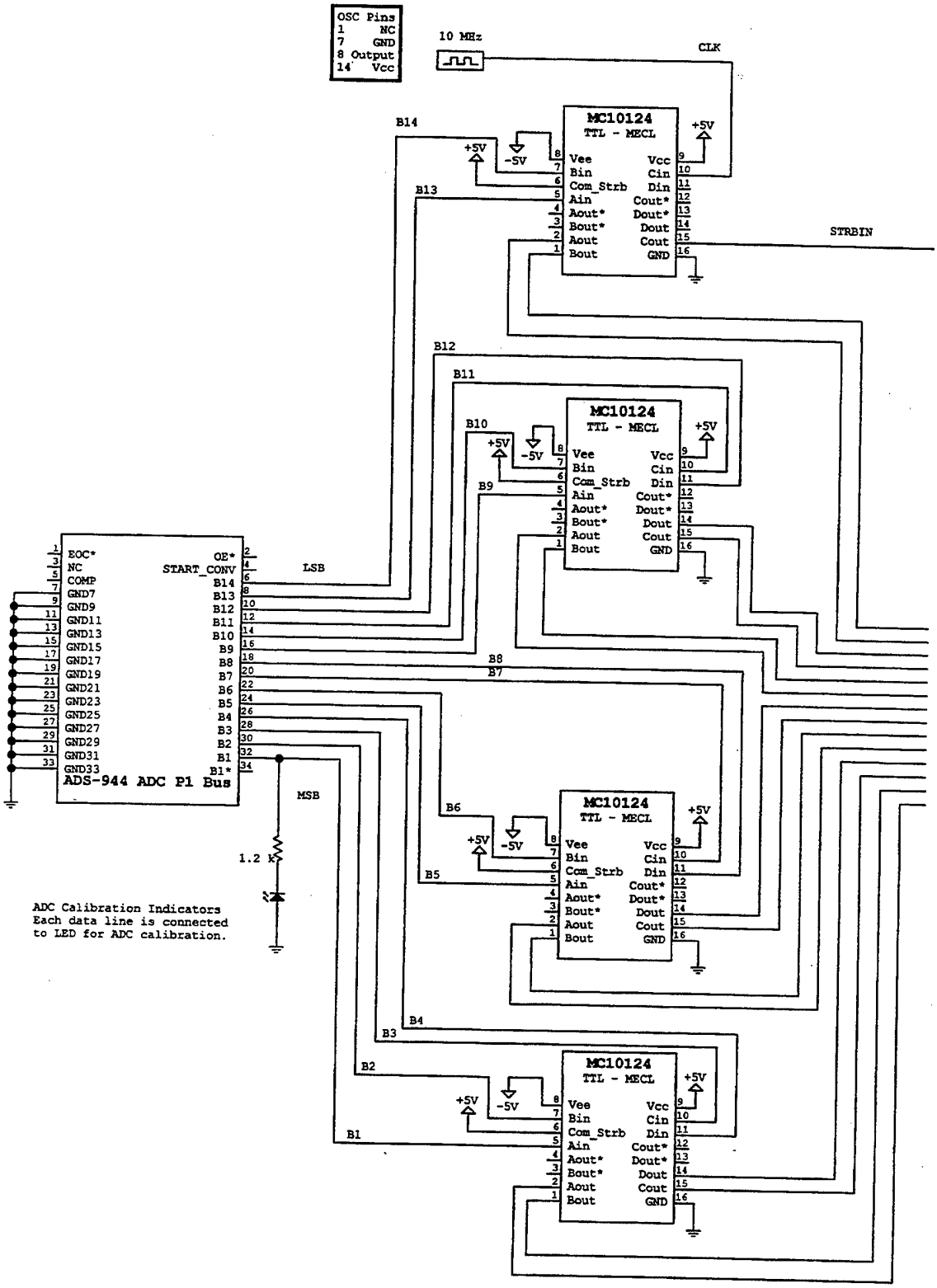


Figure 2.15(a): TX Control Board Schematic. Data Translation Section.

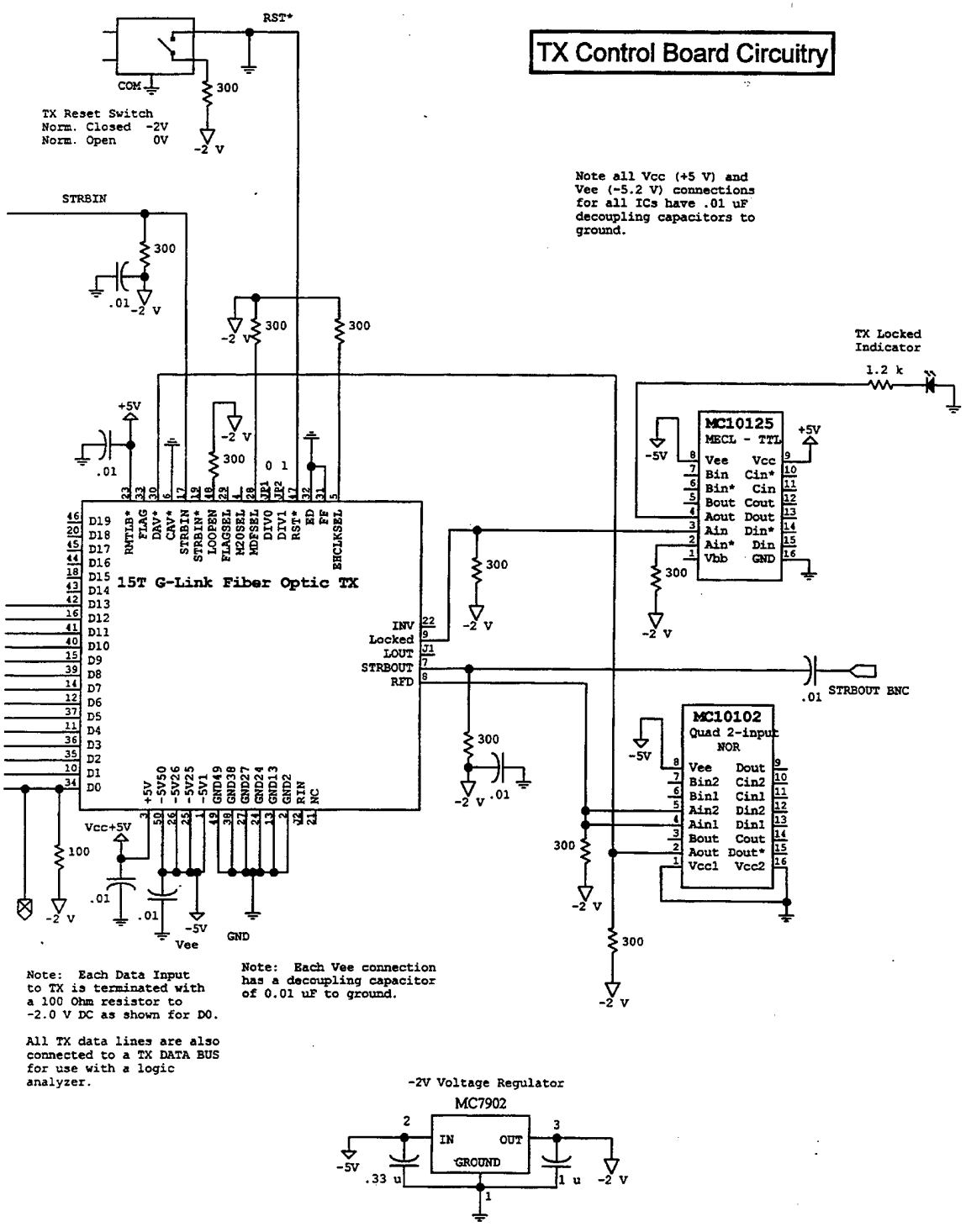


Figure 2.15(b): TX Control Board Schematic. Transmitter Module and Voltage Regulation Section.

The TX Locked signal indicates the lock status of the TX phase-locked loop (PLL). The STRBOUT signal provides an indication of the transmitter's frame rate clock and can be used to trigger an oscilloscope for timing analysis when using DOUT.

Several options of the 15T transmitter are not used in the simplex configuration and were disabled in the prototype. *Remote loopback* is not used in the simplex methods so +5.0 Vdc was hardwired to the active-low *remote loopback* pin (RMTLB*). No control words are required in the design since the data link is acting simply as a data pipe. This is equivalent to the data link serving only as the physical transport mechanism. Network protocol information for routing and flow control (such as in asynchronous transport mode (ATM) or TCP/IP networking) is handled external to the data link. In light of this, the *control word available* input (CAV*) was disabled by being tied to digital ground. *Loop enable* (LOOPEN) was tied low to enable the transmitter optical output. Should this input be asserted, the data would be transmitted via the coaxial cable output DOUT. *Double-frame mode select* (MDFSEL) was tied low to operate the transmitter in single frame mode. This option is normally used in Serial-HIPPI implementations to provide up to a 42-bit bus width. Enabling MDFSEL will only serve to cut the maximum throughput in half in the simplex data link design. The *enable data* (ED) input was tied to digital ground to always enable the transmitter to send data. *Fill frame select* (FF) was also tied high to digital ground to enable DC balanced fill frames to be sent during link synchronization. Setting this to a low value makes the transmitter send only an unbalanced fill frame (the FF0 type). *EHCLK enable* (EHCLKSEL) was tied low to use the internal variable control oscillator (VCO) of the transmitter for the transmit serial clock.

STRBIN, the *data clock input*, is generated from a 10 MHz TTL crystal oscillator which is converted to an ECL clock by an MC10124 converter. The data clock input is then connected to the active-high STRBIN input of the transmitter with a 300 Ω pull-down resistor to V_{TT}. STRBOUT, the *frame-rate data clock output*, is a frame rate clock derived from STRBIN. The frame-rate data clock takes into account the C-Field control bits of the

information frame. Input data (D0..D19 and FLAG) are latched on the rising edge of STRBOUT. Using the 5 MHz ADS-944 ADC, each input data word was transmitted twice. This allows the input data to be transmitted above the minimum 7.5 Mword/sec parallel word rate of the 15T module. This need for redundancy can be removed by using a 10 MHz electronic ADC or the electro-optic ADC being developed at NPS. A locked indication (Locked) is provided to indicate the transmitter's PLL is locked onto the data clock input. The Locked signal is routed through a MC10125 ECL-TTL converter to an LED indicating the PLL's status. Note the active low data clock input (STRBIN*) is not connected internally as configured by the manufacturer.

Data available (DAV*) input is controlled by inverting the *ready for data* (RFD) output line. RFD is a re-timed version of the ED input. The ED input is driven by the receiver state machine in full-duplex configurations. Here in the simplex configuration ED is fixed. An MC10102 Quad 2-input NOR gate is used to invert RFD and drive DAV*. The DAV* and RFD lines must have pull-down resistors to V_{TT}.

Two transmitter control inputs to the transmitter module were not connected. The *flag bit mode select* (FLAGSEL) and *16/20-bit mode select* (M20SEL) lines were left as no connects. Internal pull-down resistors in the transmitter module hold these values to ECL logic zero. With this configuration, the transmitter will operate using the flag bit (the frame's master transition) as an extra error detection bit and will operate in 16-bit mode. Leaving these connections on the transmitter modules pin package unsoldered both operates the transmitter in the desired 16-bit mode (providing enough data lines for the 14-bit data words) and allows for future increases in the data word size. Should additional data word resolution be required in the near future or should support for a variable data word size be required, electrical connections can easily be made to these pins on the prototype. The only drawback to leaving pins on the 15T/R modules as *no connects* is that adjacent pins with a very high frequency signal may interfere with the unconnected pins. No adverse effects were observed by leaving the FLAGSEL and M20SEL lines as *no connects*.

Lastly, two MC7902 –2.0 Vdc voltage regulators are included on the prototype transmitter board. Two MC7902 voltage regulators were used on the board to minimize V_{TT} connection line lengths and to minimize supply ripple voltage. A single MC7902 can supply up to 1 A of current. More details regarding the MC7902 are found in Appendix A.

This chapter described the design details for the multi-channel, high-speed, fiber-optic digital data link. Chapter III specifies the design of the data link's receiver subsystem.

III. RECEIVER SYSTEM DESIGN

A. RECEIVER SYSTEM CONCEPTS

Ideally, the receiver system is nothing more than a system which does the inverse operations of the transmitting system. The data link receiver system must: (1) recover a timing (clock) signal from the received serial data stream, (2) convert the serial data into parallel binary words, and (3) relay the binary words to the subsequent signal processing system. The serial data stream is received via an optical fiber link connected to the optical receiver. The serial data rate can be in excess of 1 Gbps. This high-speed serial data stream must be divided into the 14-bit data words used in the high-resolution digital antenna system. A functional block diagram of the electro-optic receiver system is depicted in Figure 3.1.

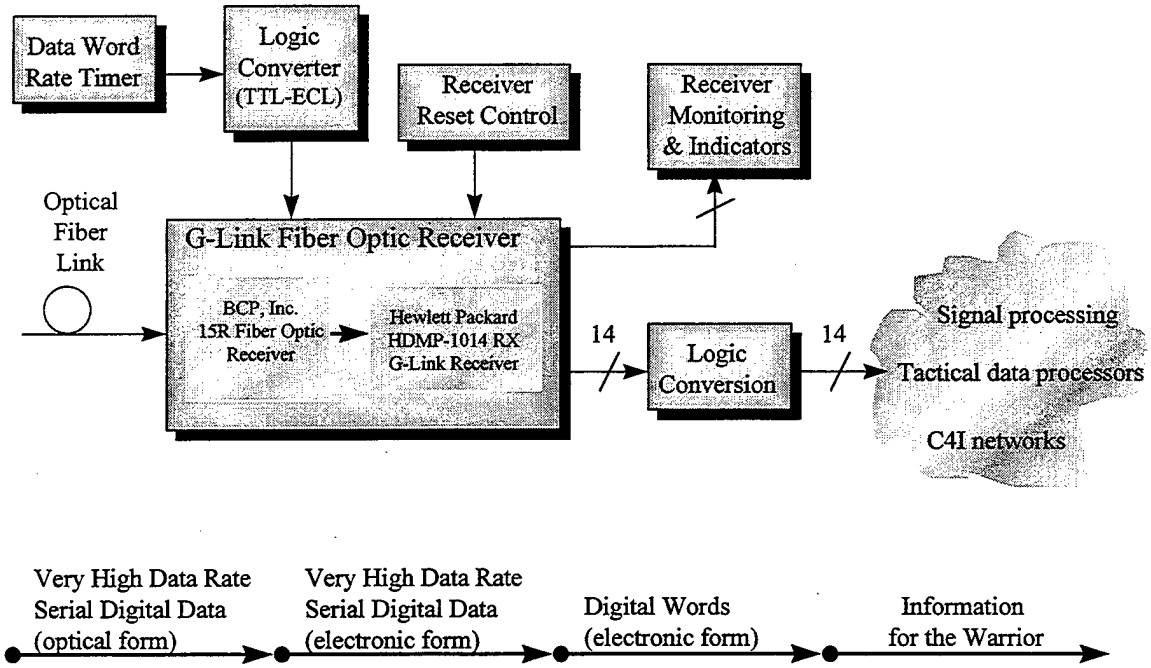


Figure 3.1: Functional Diagram of the Electro-Optic Receiver System.

In the high-speed, multi-channel, fiber-optic digital data link, the HDMP-101X series G-Link Chip Set and the BCP 15T/R optical transmitter-receiver pair were used. Recovery of the timing signal is done by the RX module. The RX module uses a

photodetector to translate the 1310 nm lightwaves into electronic signals. A PLL is used to recover a timing reference signal from the serial input. The PLL's VCO is composed of three cascaded variable delay blocks (see Figure 3.2). The timing reference signal along with the VCO are used by the RX to recover the binary data from the serial data stream [Reference 17: p. 226]. The recovered serial data is then converted to parallel data words by the RX module. If the C-Field bits or the master transition indicate an error, the frame error signal pin is asserted by the receiver module. Following translation, the 14-bit data words may be routed to modules external to the data link. [References 8 and 14]

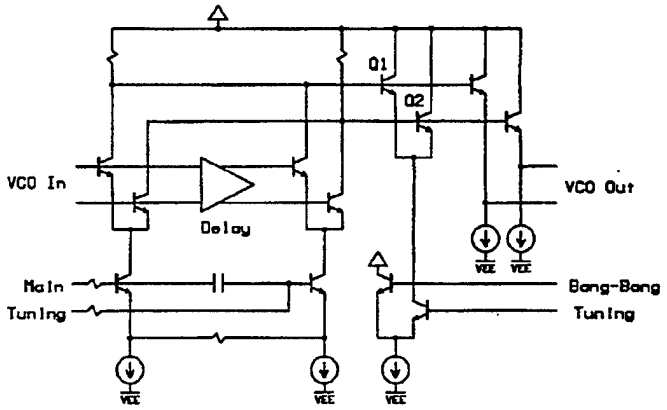


Figure 3.2: Variable Delay Block Used in Receiver's VCO [From Reference 17: p. 227].

Again the BCP G-Link set uses semiconductor photodetectors compatible with either 1310 nm or 1550 nm semiconductor lasers. The fiber lengths may be up to 1 km for multi-mode fiber and 10 km for single-mode fiber. For these fiber lengths, the receiver sensitivity is rated at –22 dBm for a bit error rate (BER) of 10^{-12}.

B. OVERVIEW OF RECEIVER SYSTEM COMPONENTS

The prototype of the high-speed data link receiver system is comprised of two primary functional sections—the BCP 15T RX module and the RX control logic. Both the RX module and the receiver control logic are mounted on a single circuit board. The receiver board is designed to interface with a subsequent signal processing board using

compatible ECL devices. Receiver functionality and device integration of the data link receiver are discussed in this section.

1. BCP 15R Gigabit Fiber Optic Digital Receiver Module

Central to the data link receiver system is the BCP 15R RX module. Consisting of the receiver portion of the Hewlett-Packard's G-Link chip set and the Broadband Communications Products Model 15R high speed serial-parallel fiber optic receiver, the module completes the point-to-point unidirectional data link.

The HDMP-1014 receiver and the HDMP-1012 transmitter have full-duplex and simplex configurations. The Simplex III configuration was used in the high-speed data link design of this thesis. A more detailed description of the link configurations is found in Chapter II and also in the Hewlett-Packard G-Link Application Note (Reference 14).

Functionally, the HDMP-1014 RX does the following: (1) recovers the timing (clock) signal, (2) recovers data from the received signal, (3) demultiplexes the serial data into parallel words, (4) decodes the data and control frames, (5) synchronizes frames, (6) detects errors in frames, and (7) controls the RX state machine. In the Simplex III configuration, the RX operates (1) by using phase differences to determine the data stream frequency (requires a phase/frequency detector, a loop filter, a variable controlled oscillator, and a clock generator), (2) by sampling the data stream and converting the serial stream into parallel words, (3) by decoding the 20 or 24-bit frame and using error detection methods to determine if a frame is in error, and (4) by sending the decoded data word to an external module through the 20 data pins and the FLAG pin. A functional block diagram of the HDMP-1014 RX is shown in Figure 3.3.

The CAV* (Control Word Available) and DAV* (Data Word Available) control lines tell the user whether the word on the data lines is a control word or data word. This feature allows the data link to differentiate between data and control information which is

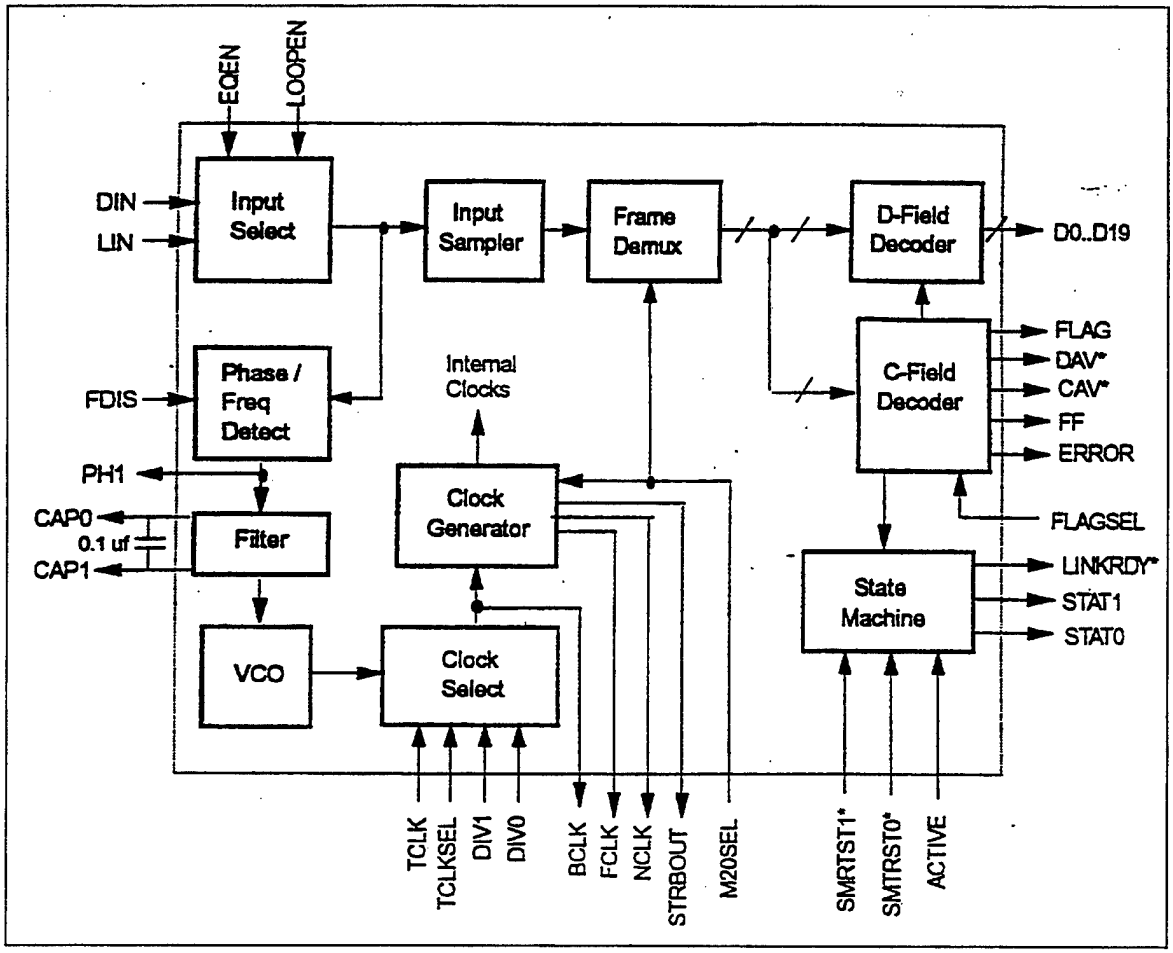


Figure 3.3: Functional Diagram of HDMP-1014 RX [From Reference 14: p. 8].

beneficial for using data link protocols such as Internet Protocol (IP) or Serial-HIPPI . The FLAGSEL control line determines whether the FLAG bit is used as an additional data line (which would provide 17 or 21 bit words) or if it is used as an additional error detection bit. When used as an error detection bit, the FLAG bit differentiates between even and odd frames. The C-Field describes the frame type (data, control word, fill frame) and is used for error detection. The D-field is nothing more than the data or control word information bits. The *frame demultiplexer* separates the C-Field and D-Field information and routes them to the appropriate decoder. *Input select* determines whether the serial input is received via coaxial cable (LIN) or optical fiber (DIN). In the Simplex III configuration, input is received through optical fiber. The *input sampler* is the device which samples the serial data and converts the data into parallel frames. The *state machine* is used in the full-duplex

configuration to perform link startup, link maintenance, and error checking. It is only used for RX module reset in Simplex III.

As mentioned in Chapter II, the Simplex III configuration requires a reference crystal oscillator to function correctly. In this design, the oscillator is a TTL-compatible 10 MHz crystal. The frequency of the reference oscillator must have at least a 0.00001 frequency difference with the transmitter's reference oscillator. Failure to meet this requirement will prevent the receiver's PLL from acquiring the timing reference signal. Reference oscillators which exceed a 0.001 frequency difference will cause an excessive time period for the receiver's PLL to acquire lock on the transmitter's signal. Severe mismatches in reference clock frequency could impair the receiver from locking onto the transmitter's signal. [Reference 14: pp. 34-35]

C. DESIGN DETAILS

With the Simplex III configuration, a prototype RX control board was designed and built to configure the 15R RX module, to conduct data link data analysis, and to provide a data interface to external modules such as a signal processing system or a computer system. The control board consists of the 15R Fiber Optic Receiver Module, assorted control logic, and error analysis logic.

1. RX Control Board

The RX control board (Figure 3.4) receives serial data via an optical fiber link connected to the TX control board. The optical data stream is converted into a 14-bit binary word by the 15R RX module. The received data is then latched on the rising edge of the receiver's STRBOUT clock signal. A logic analyzer was used to monitor the received data and compare it to the transmitted data words. Data lines are available for interface with an external ECL-compatible module such as the logic analyzer or a signal processing board. Due to the nature of the receiver's 100K ECL data output lines, connections between the RX data output lines and subsequent digital devices should be kept as short as possible (less

than 2 inches, if feasible). Output data lines that are longer will require the use of transmission line techniques described in ECL transmission line theory (refer to Reference 19 and Appendix B).

Received data is routed through the D0..D19 and FLAG pins of the receiver module. Since only 14-bit data words were implemented in this design, only the D0..D13 lines were connected with 300 Ω pull-down resistors to V_{TT}. Each data line should be kept as short as possible due to adverse transmission line effects. MC10176 D flip-flops were used to latch the receiver module's data lines. Data was latched on the rising edge of the RX STRBOUT signal. Damping resistors of 150 Ω (used to match the characteristic impedance Z_o of the transmission line) were placed in series with the data line outputs to increase the acceptable line length to drive the flip-flops. Figure 3.5 illustrates the use of series damping resistors (R_D) with pull-down resistors (R_P). Unused data lines (D14..D19 and FLAG) may be left as *no connects* with no adverse consequences. Data line D0 is the most significant bit of the data word. V_{EE} connections to the 15R module and all ECL devices are decoupled with 0.01 μF capacitors to ground. Ground connections were as expected. Note that V_{CC} voltages vary depending upon device type.

The data clock reference signal is generated by the TTL 10 MHz crystal oscillator whose output is converted to ECL with an MC10124 TTL-to-ECL converter. Note that V_{CC} and the common strobe (Com_Strb) must both be tied to +5.0 Vdc on this device since digital ground applied to Com_Strb will invert the converted TTL signal. The generated ECL clock signal requires a pull-down resistor (300 Ω) to V_{TT}. A filtering capacitor of 0.01 μF is used here. In the Simplex III configuration, this reference clock signal is routed through the local loopback data connection (LIN). LIN is a buffer-line logic (BLL) MMCX coaxial connection. BLL requires the input signal to be AC coupled. Therefore, the reference clock signal was passed through a DC-blocking 0.1 μF capacitor which generates a reference clock signal swinging around digital ground.

In the full-duplex configuration, the *state machine status inputs* (SMRST0* and SMRST1*) are used to control the initial start-up sequence and receiver reset. Here the simplex design only requires the receiver active low reset signal (RST*) be tied to the SMRST0* and SMRST1* pins. Just like the transmitter control board, a momentary push-switch was used on the prototype receiver control board to enable RST*. The *normally open* position is tied to digital ground and the *normally closed* position is tied to ECL logic low through a pull-down resistor to V_{TT}.

Inputs *frequency detector disable* (FDIS) and *chip enable* (ACTIVE) are driven by the receiver's state machine status output STAT1. STAT1 controls these inputs to properly synchronize the link start-up sequence and normal data recovery. When FDIS is active, the RX PLL frequency detector is disabled and a phase detector is enabled. The phase detector is used to receive data patterns over the link. The PLL frequency detector is used during the start-up sequence to acquire wide-band lock on fill frames. ACTIVE is internally retimed by STRBOUT. It is then presented by the RX module as the LINKRDY* signal. LINKRDY* indicates the receiver's start-up sequence is complete. An MC10102 quad 2-input NOR gate is used to invert the STAT1 signal. It is routed to the *local loopback control* (LOOPEN) input. LOOPEN determines if the LIN input is used vice the optical fiber input. In the Simplex III configuration, LIN receives the 10 MHz input strobe clock. [Reference 8: pp. 15-16]

The *link ready indicator* (LINKRDY*) is tied together with the *data available* (DAV*) output. The two outputs are tied together to eliminate the possibility of false data indications during link initialization. In the receiver board schematic (Figure 3.4), the LINKRDY*/DAV* combination is latched by an MC10176 flip-flop. The indication signal

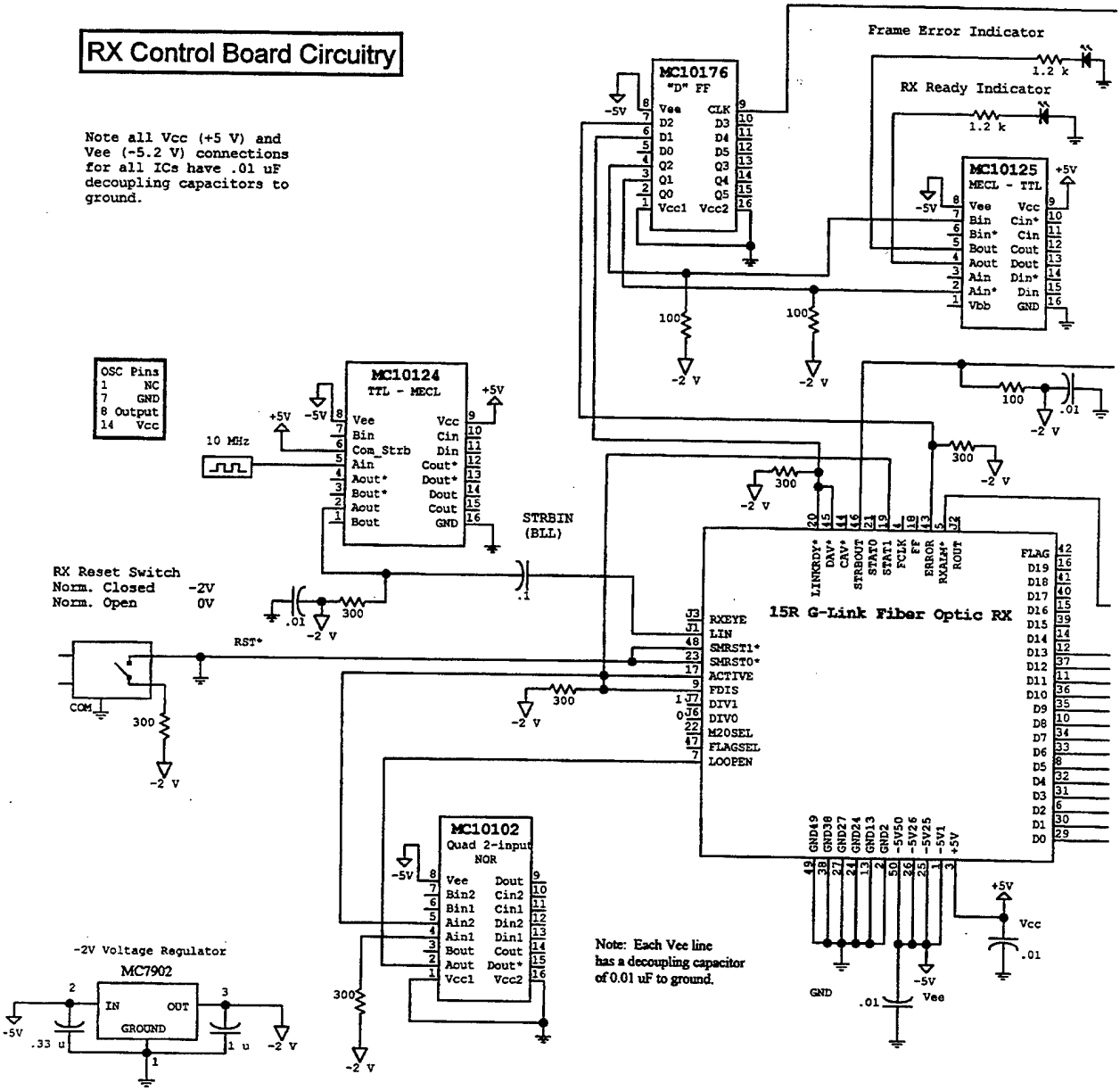


Figure 3.4(a): RX Control Board Schematic.

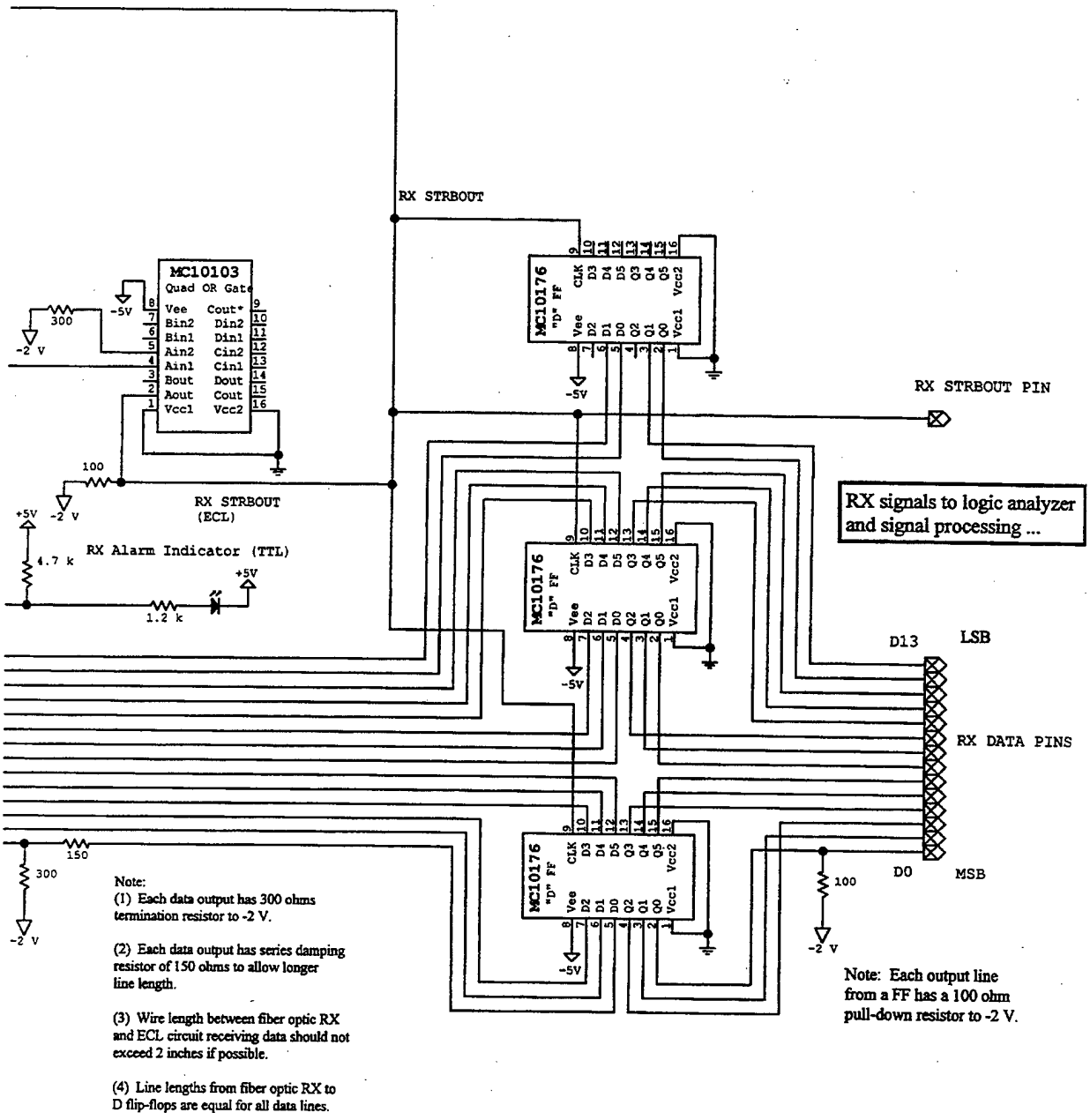


Figure 3.4(b): RX Control Board Schematic.

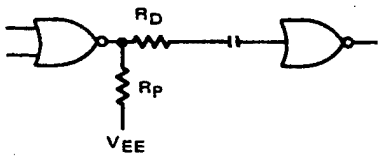


Figure 3.5: Series Damping and Pull-Down Resistors Used Between ECL Gates [From Reference 19: p. 27].

is then routed to an MC10125 TTL-MECL converter and an LED. *Control word available* (CAV*) output is not used in this design since the link is acting solely as a data pipe.

STRBOUT, or the recovered frame-rate data clock output, is used to latch D0..D19, FLAG, DAV*, CAV*, FW, LINKRDY*, and ERROR. The rising edge of STRBOUT indicates when these signals should be latched. An MC10103 quad OR gate was used to output the recovered RX frame-rate data clock. STRBOUT can only effectively drive one ECL gate. Using the intermediate OR gate allows the STRBOUT signal to be routed to four MC10176 flip-flops latching the output data lines and control signal outputs. The MC10103 can drive four 10K ECL gates with no fan-out problems. Clock skew in the RX STRBOUT clock signal is not a problem since only four flip-flops are being clocked. Should more flip-flops be required in a future design (e.g., increasing the word size beyond 18 bits), a more complex clock distribution network will have to be employed. The method is described in References 18 and 19.

FLAGSEL and M20SEL are left as no connects as discussed in Chapter II. So long as no high frequency signals adjacent to these pins interfere, the link will function correctly and allow future ADC data word resolution enhancement.

Receiver alarm (RXALM*) indicates either receiver failure or low optical input power. RXALM* is an open collector TTL signal requiring a 4.7 kΩ pull-up resistor to TTL V_{CC}.

In Chapter III, the receiver subsystem of the multi-channel, high-speed, fiber-optic digital data link has been described. Now all the data link components and their functions

have been illustrated for the reader. Chapter IV details the testing and evaluation of the data link. The following chapter provides a comparison with two other data link designs for military applications and recommends some design improvements. Chapter VI lists the author's conclusions and recommendations for further study.

IV. TESTING AND EVALUATION OF THE DATA LINK

Following design and implementation of the multi-channel, high-speed, fiber-optic digital data link, testing and evaluation was required to verify the prototype met or exceeded the design goals as specified in Chapter I. The testing and evaluation was divided into three phases: (1) a data link requirements evaluation, (2) link testing and performance evaluation, and (3) an assessment of observed design and/or operational problems. The data link requirements evaluation phase appraised the data link's power, thermal, and optical fiber link requirements. Additionally, all components were tested to verify that appropriate signal levels were applied for proper link operation. Next the data link's performance was evaluated by testing the data link using the ADS-944 ADC. Both variable and fixed voltages were used to generate binary test patterns for transmission through the data link. Transmitted and received data were compared for correct link operation and data errors. Lastly, any observed design flaws, pitfalls, or concerns were noted. These design problems are listed in the last section of this chapter.

A. DATA LINK REQUIREMENTS EVALUATION

Initial evaluation of the data link included the ADC control board, the ADS-944 evaluation board, the transmitter board, a 5.5 m single-mode fiber optic link, the receiver board, power supplies, a function generator, an oscilloscope, and a logic analyzer. All board designs are the same as were described in Chapters II and III.

1. Data Link Power Requirement Evaluation

To insure correct operation of the data link, proper power supply distribution is a must. Most of the TTL and ECL devices which implement the transmitter and receiver's control logic are fairly flexible with regard to power supply deviations. BCP 15T/R modules require power supply voltages be within a +/– 5% tolerance. For proper link operation, the user must verify that the V_{CC} and V_{EE} supplies provide voltage regulation

within these limits. As designed, MC7902 voltage regulators were used on the TX and RX boards to provide the proper V_{TT} potential from the V_{EE} supply.

ECL devices require a relatively large amount of current when compared to other logic families such as TTL or CMOS. This is due to the bipolar transistors steering current to achieve high-speed logic transitions. Most power supplies common in our digital laboratories are designed for use with the lower-power TTL and CMOS families. These supplies typically offer a 5 volt supply with a maximum current rating of 1 A while the variable supplies are rated at 0.25 to 0.5 A. When the supply current approaches the maximum current rating, variations in the power supply regulation can effect supply voltages. BCP 15T/R modules each require near 1 A for their V_{EE} supplies. To meet the ECL current requirements, power supplies rated at 2 A or greater were used for the V_{EE} supplies for the transmitter and receiver boards. Table 4.1 lists the maximum required operating current versus measured operating current of the data link circuit boards. [Reference 8: p. 9]

	Current Requirements in mA maximum required (measured)			
Circuit Board	**+5 Vdc (V_{CC})**	**–5 Vdc (V_{EE})**	**+15 Vdc**	**–15 Vdc**
ADC Boards	451 (431)	200 (158)	80 (46)	80 (57)
ADC Control Board	181	0	0	0
ADS-944 Board	270	200	80 (46)	80 (57)
Transmitter Board	420 (419)	1131 (936)	0	0
Receiver Board	287 (165)	1588 (1350)	0	0

Table 4.1: Data Link Circuit Board Current Requirements.

Based on the power requirements described in Table 4.1, V_{EE} buses for the transmitter and receiver board were supplied by power supplies capable of providing at least

2 A of current. V_{CC} buses were supplied by 1 A supplies. The ADC boards' V_{EE} bus and +/– 15 Vdc buses were supplied by 0.25 or 0.50 A supplies.

2. Data Link Thermal Requirements

ECL components and high-speed analog-to-digital converters dissipate a great deal of heat. Neglecting thermal requirements of the devices can cause the devices to fail prematurely. The 15T/R modules have built-in heat sinks to dissipate heat from these modules. All other ECL devices and the ADS-944 are not manufactured with built-in heat sinks. In an open air laboratory design such as the data link prototype, air flow and operating temperature were sufficient to dissipate the generated heat; however, in subsequent designs and in a field system, more attention will have to be paid to heat dissipation and thermal relief.

3. Fiber Optic Requirements

BCP claims their fiber optic modules will work with a minimum 1 meter cable length. However, they will not guarantee operation below 5 meters [Reference 8: p. 9]. During testing of the data link, the data link operation was verified with no intervening cable, a 1 m multimode link, and a 5.5 m single-mode link (with a 1.56 dB loss). Single-mode ST connectors were used in all links to minimize signal loss. The receiver also correctly detected loss of optical power. When optical power at the receiver end of the link falls below the receiver's sensitivity (e.g., due to loss of power in the transmitter, or disconnected or broken fiber link), the receiver asserts its receiver alarm signal (RXALM*). If RXALM* is asserted, a LED is illuminated indicating low (or loss of) optical power at the receiver.

Transmitter laser diode power was verified to be within the specified range. The optical wavelength is specified as 1310 nm +/– 20 nm. The measured optical wavelength was 1312.9 nm. Optical transmitter power is specified to be in the range of –9 to –6 dBm. The measured optical transmitter power is 117.525 μW. This corresponds to a measured value of –9.299 dBm. [Reference 8: p. 9]

B. LINK PERFORMANCE AND TESTING

In testing the data link, both fixed voltage and triangular wave signals were used as inputs to the ADC's analog input. A fixed voltage signal into the ADC results in a constant bit pattern such that each data valued latched at the receiver should be the same constant bit pattern. The triangular wave input varies the ADC's analog input over its entire input range (−1.25 V to +1.25 V). In the triangular wave (or any other varying analog input waveform), each channel will receive a varying bit pattern. A latency of two frames between data input into the receiver module to update the receiver's synchronous outputs was expected [Reference 14: p. 11]. This latency can only be observed when the input data varies.

Figure 4.1 depicts the observed STRBIN waveforms for the transmitter and receiver modules. The TX STRBIN signal (shown on the left side of Figure 4.2) is a 10 MHz ECL signal which controls the word rate at which data is converted from parallel data words to a serial bit stream. As configured, the data link produces a 200 Mbps serial data rate. Only 140 Mbps of the serial data rate carries the 14-bit words. Frame header overhead (used for frame error detection) accounts for 40 Mbps. The remaining 20 Mbps is unused data since the data link is operating in 16-bit data mode and two channels are not carrying information. On the right side of Figure 4.1, the 10 MHz buffer line logic (BLL) signal RX STRBIN swings around digital ground from −0.35 V to +0.35 V. This signal is used by the receiver module to recover timing and data signals.

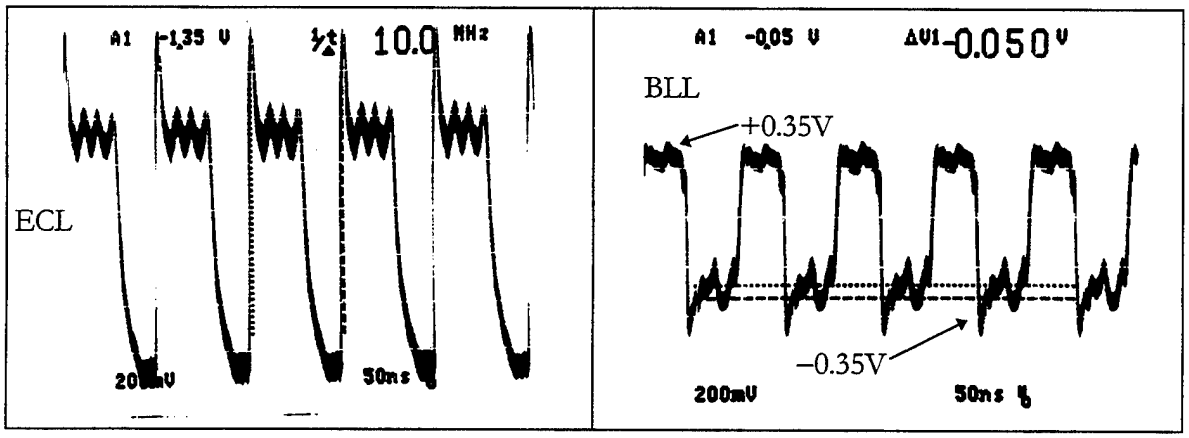


Figure 4.1: Comparison of TX and RX STRBIN.

The transmitter and receiver generate STRBOUT signals which may be used for test equipment triggering and for latching data values. In Figure 4.2, the left side displays the measured 10 MHz TX STRBOUT signal. This signal is useful for triggering test equipment to observe the serial data stream and to determine when input data is latched. On the right, the RX STRBOUT signal also has a frequency of 10 MHz. The RX signal is used to latch data outputs on the receiver and to latch control signals generated by the receiver module.

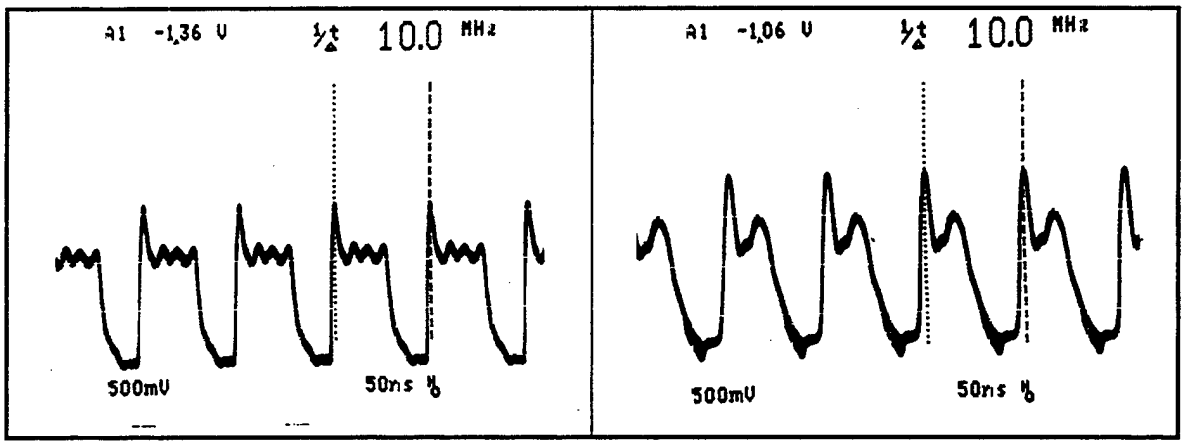


Figure 4.2: Comparison of TX and RX STRBOUT.

Ideally, an ECL pulse should have an undershoot less than 100 mV. (An ideal ECL waveform appears in Figure 4.3.) The transmitter's STRBOUT signal has an undershoot of 130 mV and the receiver's STRBOUT has an undershoot of 160 mV. Figures 4.4 and 4.5 show an individual STRBOUT pulse verses a data channel. The undershoot measurements are reflected in this figure. For a wire-wrapped prototype board, the waveform shape is good. A more noise resistant design such as a printed-circuit board (PCB) implementation should improve signal quality.

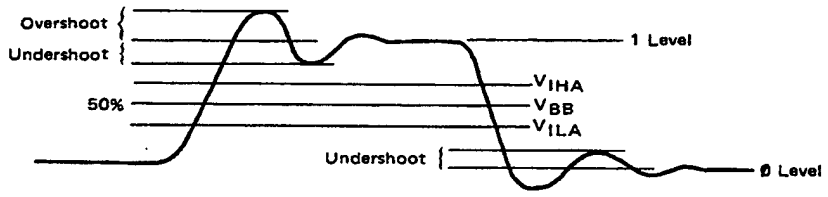


Figure 4.3: An Ideal ECL Pulse [From Reference 19: p. 64].

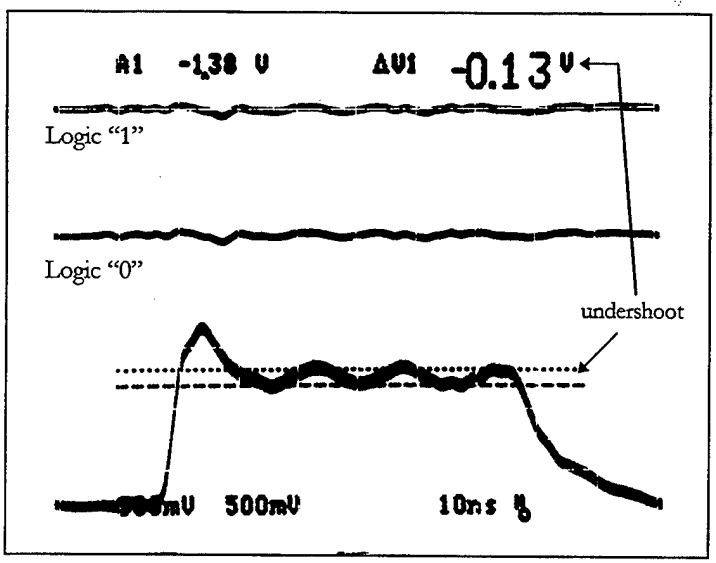


Figure 4.4: Comparison of TX Data and TX STRBOUT.

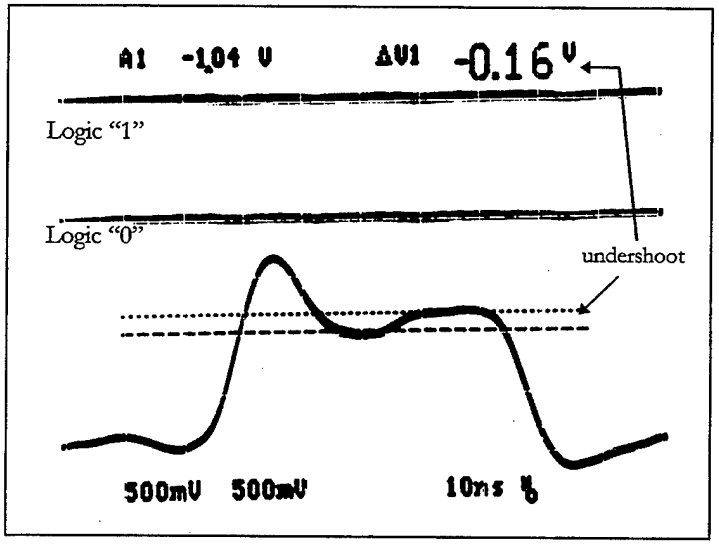


Figure 4.5: Comparison of RX Data and RX STRBOUT.

1. Constant Input Voltage Testing

To demonstrate operation of the data link, fixed voltages were applied to the analog input. Both a fixed voltage in the ADC's positive and negative voltage ranges were used as input. For the positive constant voltage test, a voltage of +0.625 Vdc was applied to the ADC's analog input. This voltage corresponds to the +½ full-scale input and should

produce a bit pattern of 11 0000 0000 0000 in offset binary. Since the ADC could not be calibrated properly (discussed in the design pitfalls section of this chapter), the ADC mistakenly produced a bit pattern of 11 0001 0111 1111 in offset binary. Several of the ADC's least significant bits (LSB) were often set to the incorrect binary pattern for the respective input voltage. While annoying, the focus of the testing using the ADC was to observe proper operation of the data link. Proper operation of the data link was observed as noted in the data figures of this chapter. The ADC's disparity between the input voltage and the output binary pattern is likely due to an improperly calibrated ADC and/or device failure within the ADC circuitry.

Figures 4.6 and 4.7 display the transmitted bit pattern and received bit pattern obtained from the digital logic analyzer's display. The signals denoted by DATA0..13 represent the data word input to the transmitter where DATA0 is the most significant bit (MSB). TXCLK is the transmitter's STRBOUT signal which is used to latch the input data lines. RXDATA0..13 represent the data word recovered by the receiver. RXCLK is the receiver's STRBOUT signal which is used to latch the received data into the receiver's registers (flip-flops). At the top of the figures are several logic analyzer status indicators. The *100/500MHz LA E* indicator means the logic analyzer is in the logic analyzer mode. *Waveform 1* indicates the display is set to view a timing waveform. The indicators *Acq. Control*, *Cancel*, *Run*, and *Center Screen* are control buttons to operate the logic analyzer. *Accumulate Off* notifies the operator that signal changes are not being accumulated over time such as in the logic analyzer's transitional mode. The *X–>* and *O–>* show the hexadecimal value under the X and O markers. These markers were used to measure time differences in the data link testing. The *sec/Div* indicator shows the current time per division setting of the logic analyzer. There are ten divisions for data on the logic analyzer display. *Delay* lists how far into the current set of captured data the user is observing. The indicated delay is for the start of the first division of the display. *Markers Time* means the X and O markers are set to measure time. *X to O* measures the time period between the two dashed markers. *Trig to X* measures the time period between the trigger marker (the dotted

line) and the X marker while *Trig to O* measures the period between the trigger and the O marker. On most of the data figures derived in the data link testing, the X to O marker was used to measure the latency between input to the transmitter and output from the receiver's data line registers. As used during the prototype testing, the logic analyzer X and O markers each have an error of +/– 10 ns.

The negative constant voltage was set to the –½ full-scale voltage of –0.625 Vdc. The correct offset binary bit pattern for this voltage is 01 0000 0000 0000. However, the ADC produced a bit pattern of 01 0001 1111 1111. Transmitted and received binary values for the negative constant voltage input are found in Figures 4.8 and 4.9. Figures 4.6 through 4.9 clearly demonstrate that the transmitted bit pattern corresponds to the received bit pattern for a constant voltage input. Transitions between constant voltage levels by manually adjusting the applied constant voltage input could not be captured by the logic analyzer. However, the varying voltage input tests in the next section clearly show these transitions.

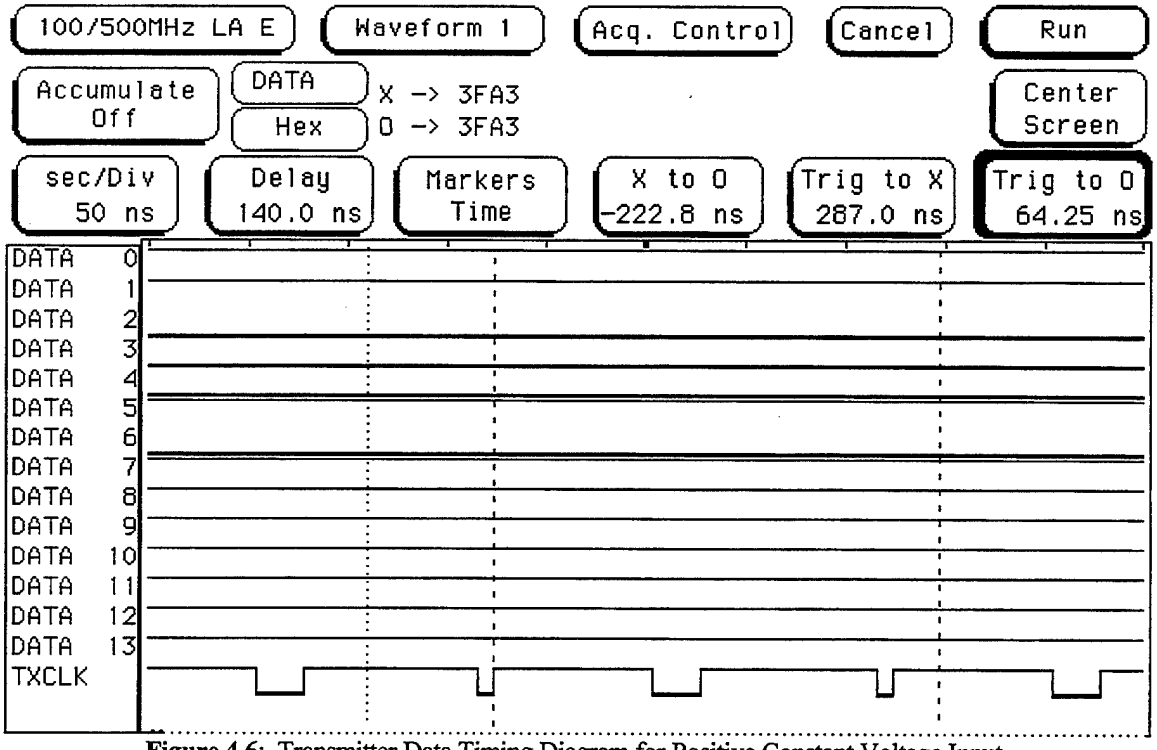


Figure 4.6: Transmitter Data Timing Diagram for Positive Constant Voltage Input.

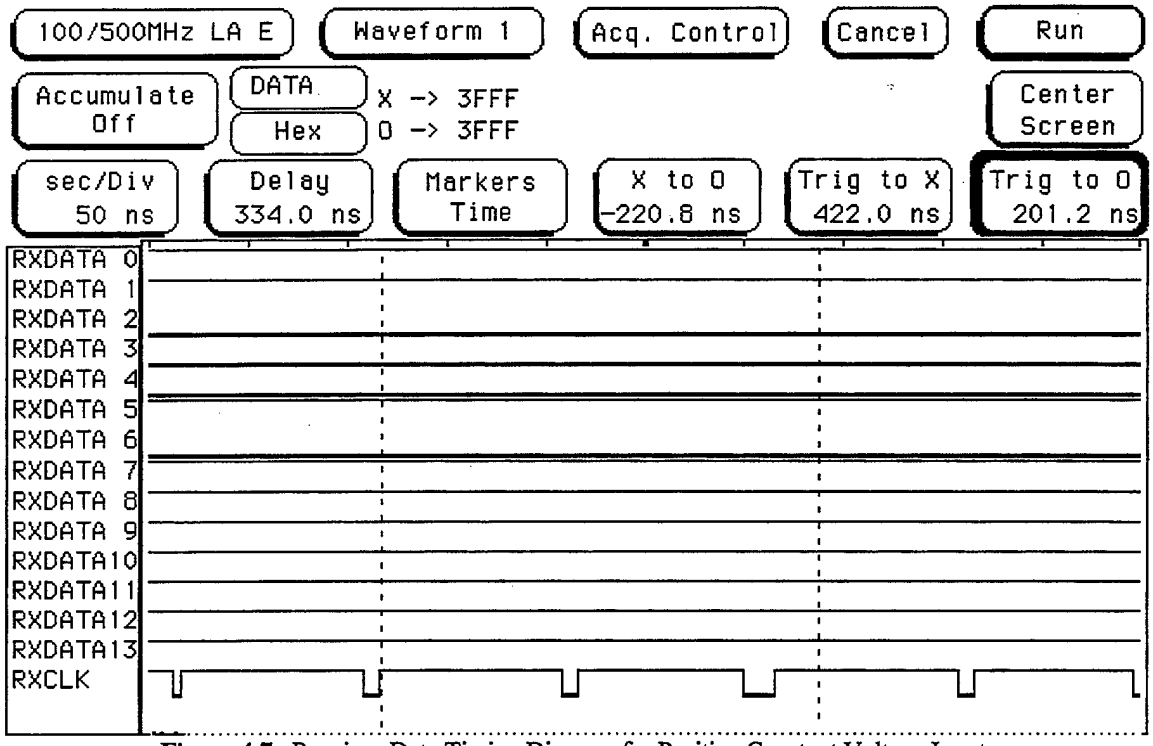


Figure 4.7: Receiver Data Timing Diagram for Positive Constant Voltage Input.

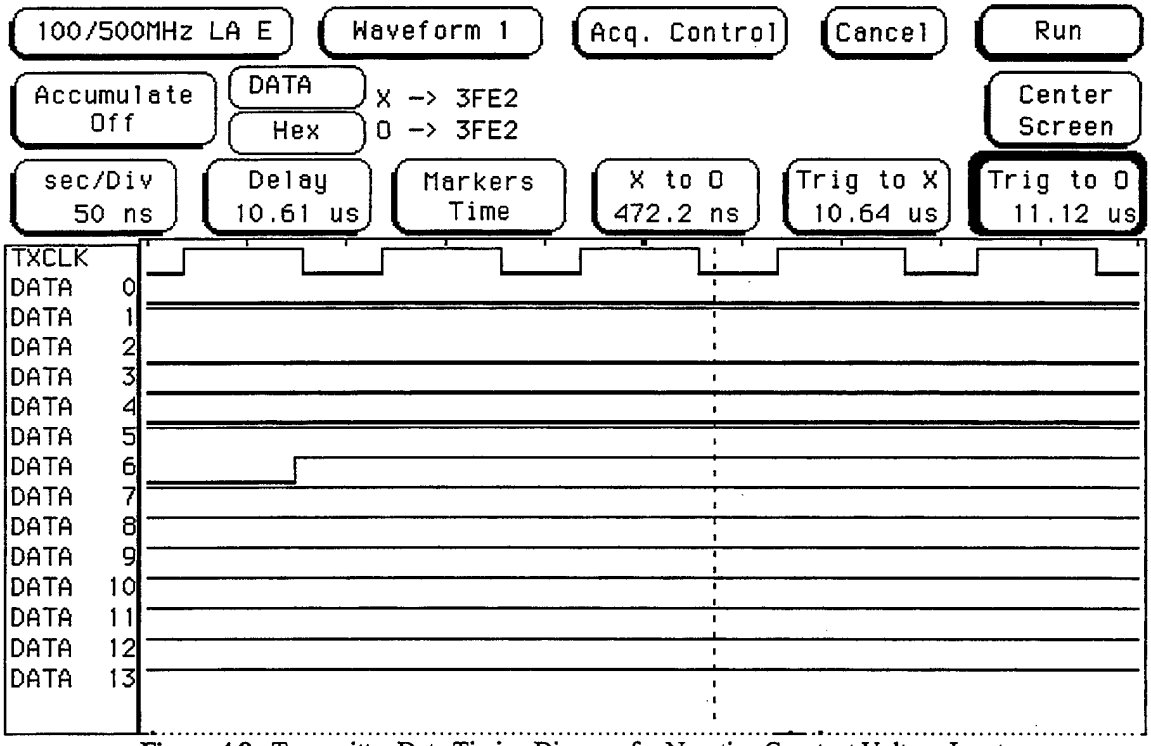


Figure 4.8: Transmitter Data Timing Diagram for Negative Constant Voltage Input.

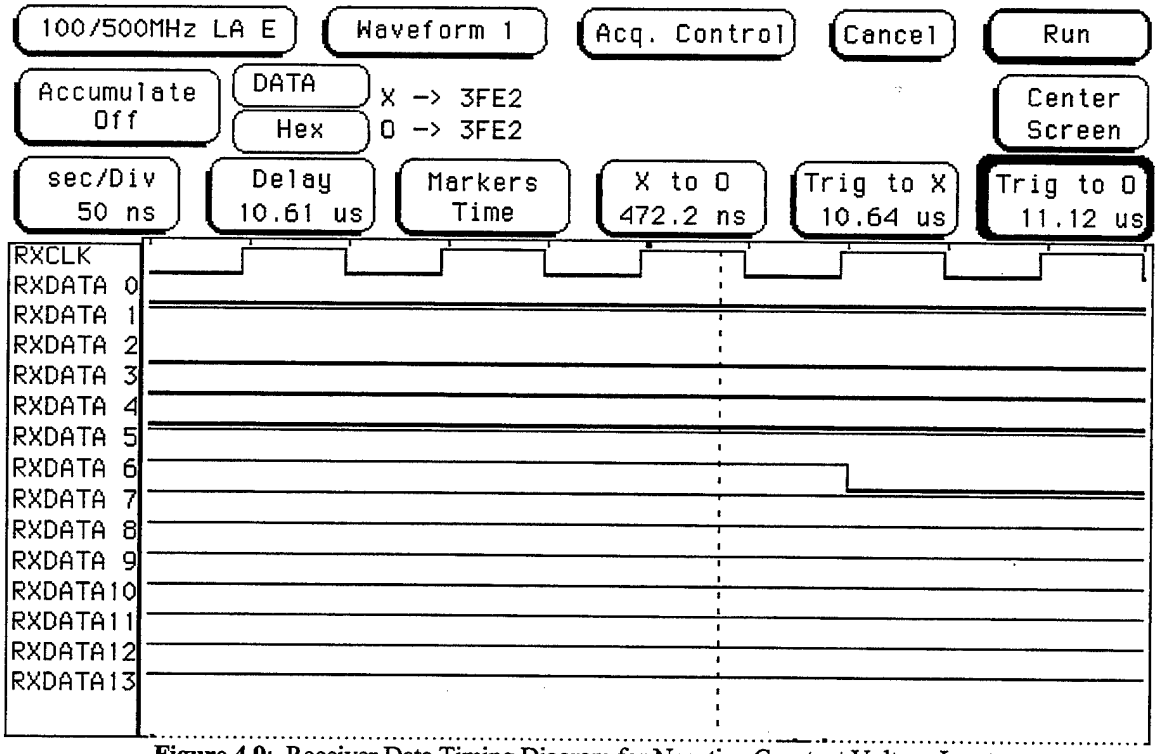


Figure 4.9: Receiver Data Timing Diagram for Negative Constant Voltage Input.

Serial data for both the positive and negative ½ full-scale voltages appear in Figures 4.10 and 4.11. These figures show the serial transitions triggered by the STRBOUT pulse. Eye pattern analysis may be used to analyze the signal quality of the serial data (i.e., timing jitter and noise). A more detailed explanation of eye pattern analysis is found in Reference 10. Figure 4.12 illustrates the points of interest in such analysis. T_b is the bit period for the serial data. Point A is the noise present for a logic "1" and point B is the noise present for logic "0." The width of the threshold crossing (Point C) determines timing jitter. Serial data for constant voltage input displays little noise and some timing jitter for the 200 Mbps data rate. T_b was measured to be approximately 4.9 ns. For 20-bit frames, this equates to a 10.2 Mword/sec measured parallel data rate. [Reference 10]

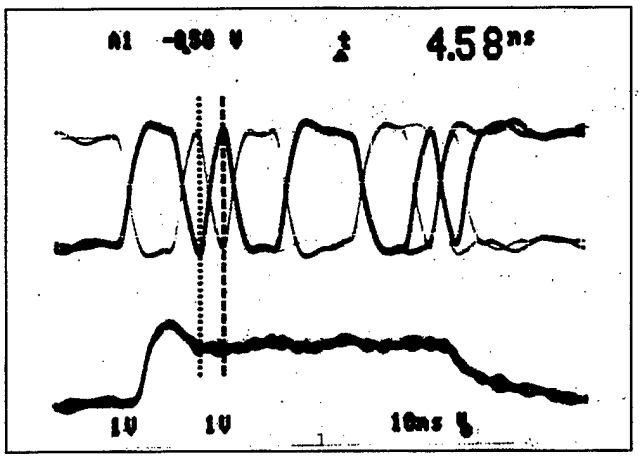


Figure 4.10: Eye Pattern Analysis of Transmitted Serial Data for Positive Fixed Input.

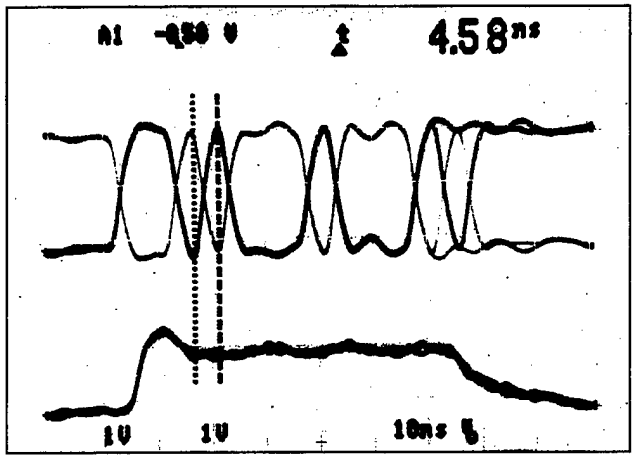


Figure 4.11: Eye Pattern Analysis of Transmitted Serial Data for Negative Fixed Input.

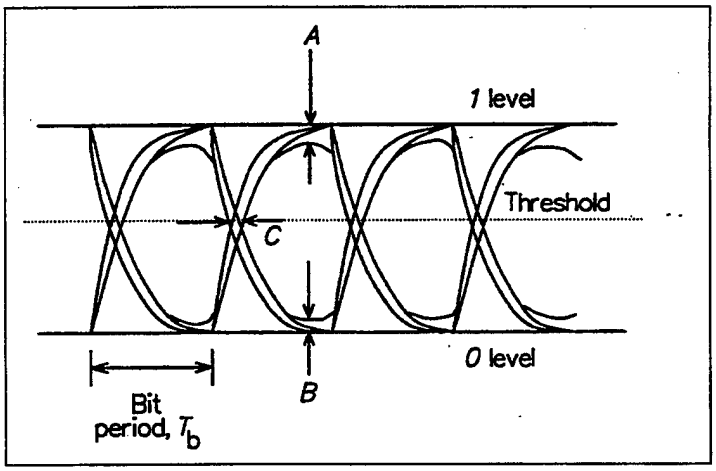


Figure 4.12: Representative Eye Pattern Analysis of High-Speed Serial Data [From Reference 10: p. 202].

2. Variable Voltage Input Testing

Variable voltages were applied to the ADC analog input to test link performance over the entire ADC input range (–1.25 V to +1.25 V). A triangular wave was used as the input signal (see Figure 4.13). The data link was tested with input signal frequencies of 10.1 kHz, 101.0 kHz, 1.01 MHz, 2.06 MHz, and 10.1 MHz. For the 5-MHz sampling ADC used to process the input signals, the first four signals fall below the Nyquist rate. The 10.1 MHz input will produce an aliased signal. In the prototype data link, actual signal content is unimportant in testing the data link. The primary concern is that the receiver generates the same binary pattern which is transmitted to it. Secondly, the variable voltage input testing provided an estimate of the latency of the data link.

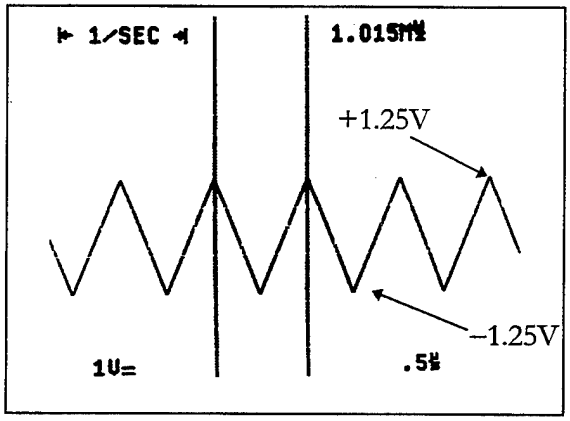


Figure 4.13: 1.015 MHz Triangular Wave ADC Analog Input.

In the first test case (10.1 kHz triangular wave input), the transmitted binary patterns for the transmitter data lines are shown in Figure 4.14. Received binary patterns are found in Figure 4.15. Observe that the transmitted data pattern appears on the receiver data lines after a small delay (refer to point ❶ in the figure). This delay is the time between applying the input signal to the 15T fiber optic module and reading the received signal at the receiver board's flip-flops. In Figures 4.16 and 4.17, we see the delay measured on different channels is consistent. In this test case, the measured latency was 502.2 ns.

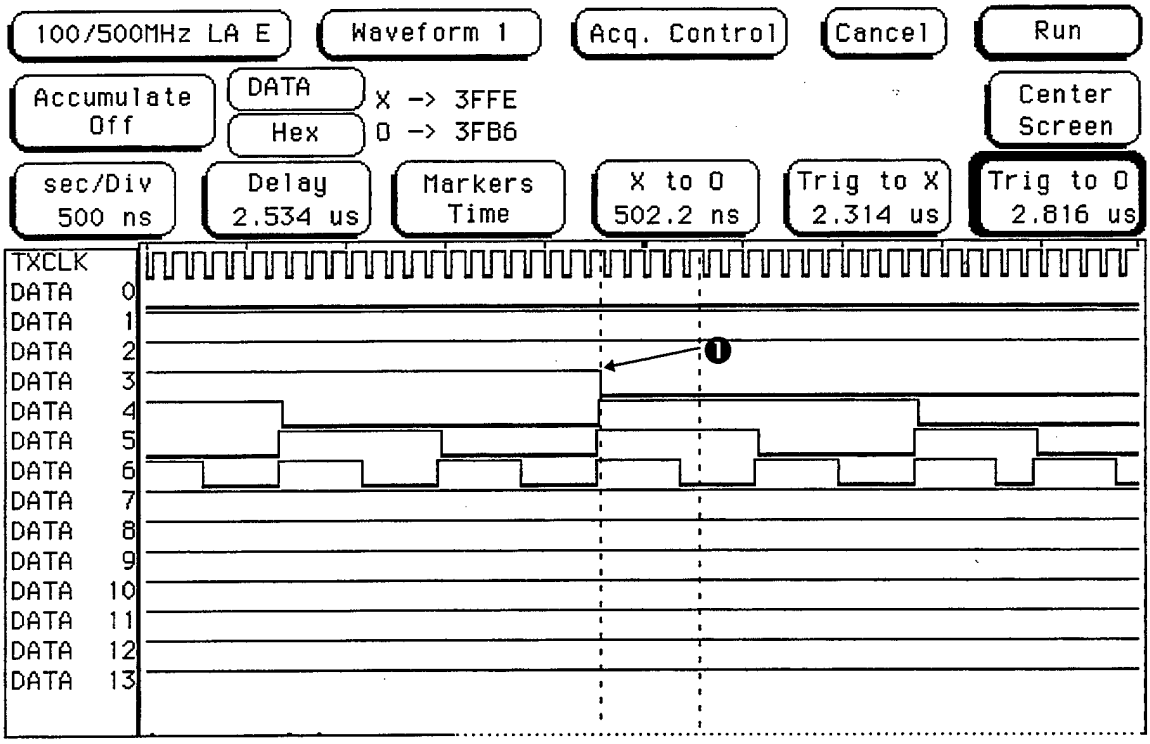


Figure 4.14: Transmitter Data Timing Diagram for 10 kHz Triangular Wave Input.

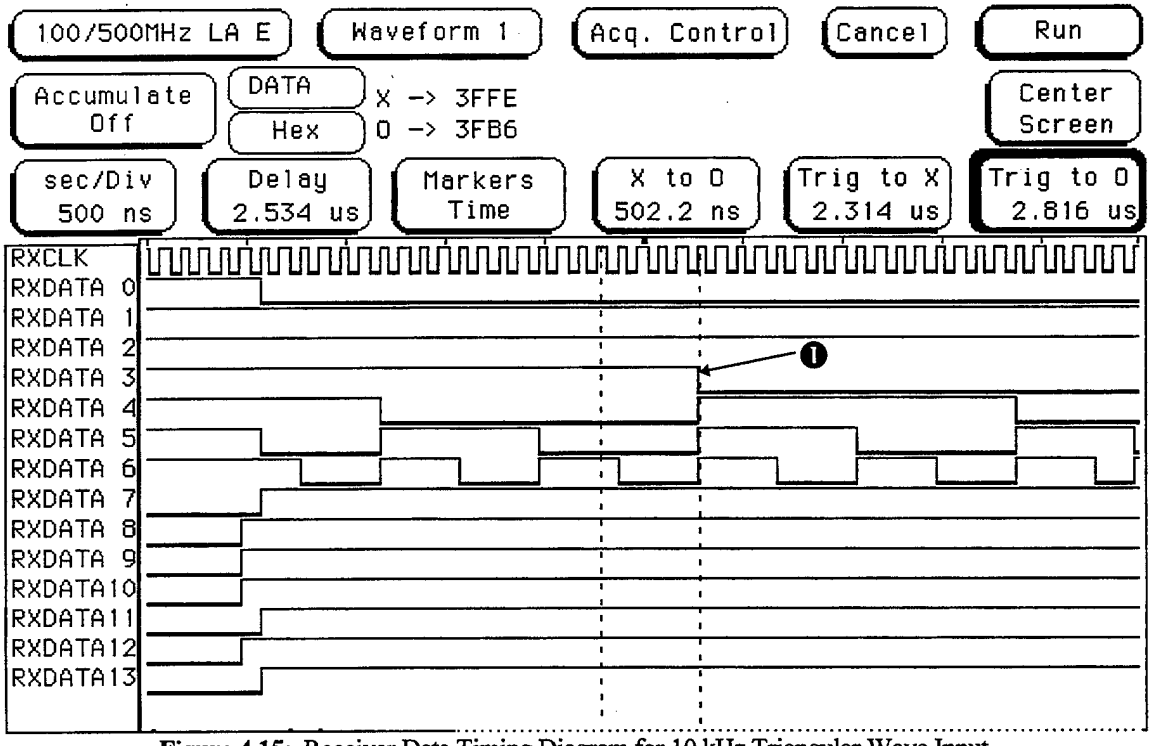


Figure 4.15: Receiver Data Timing Diagram for 10 kHz Triangular Wave Input.

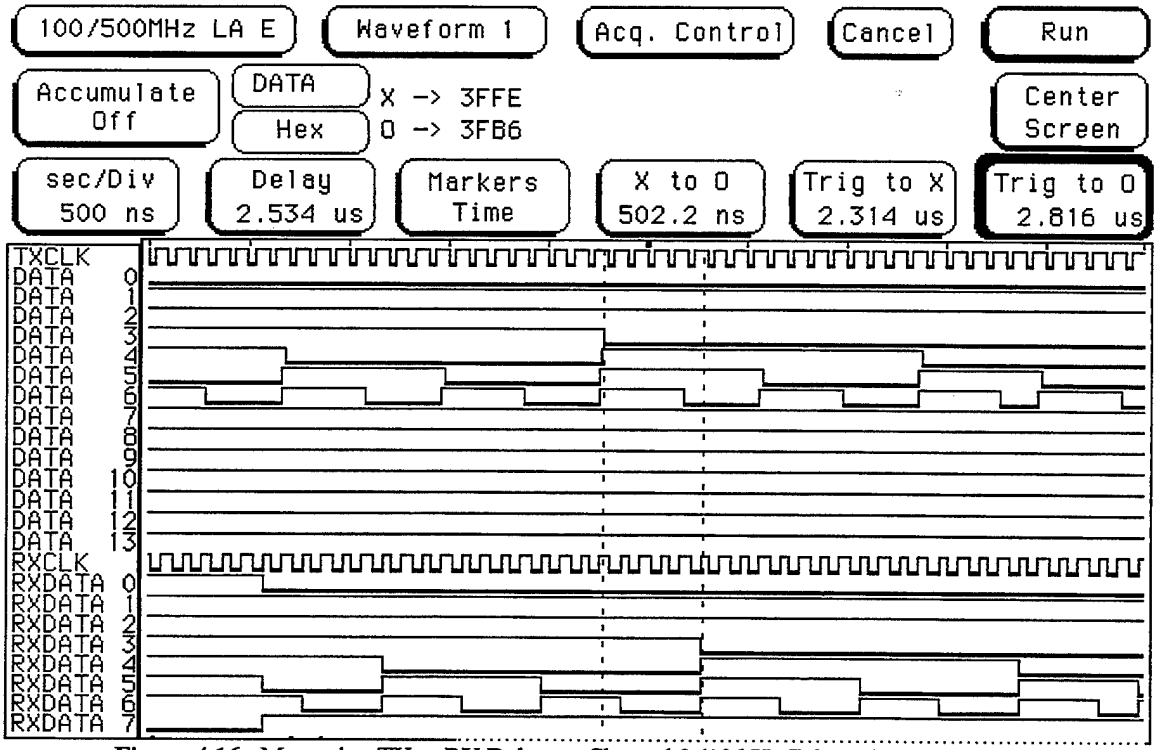


Figure 4.16: Measuring TX to RX Delay on Channel 3 (10 kHz Triangular Wave Input).

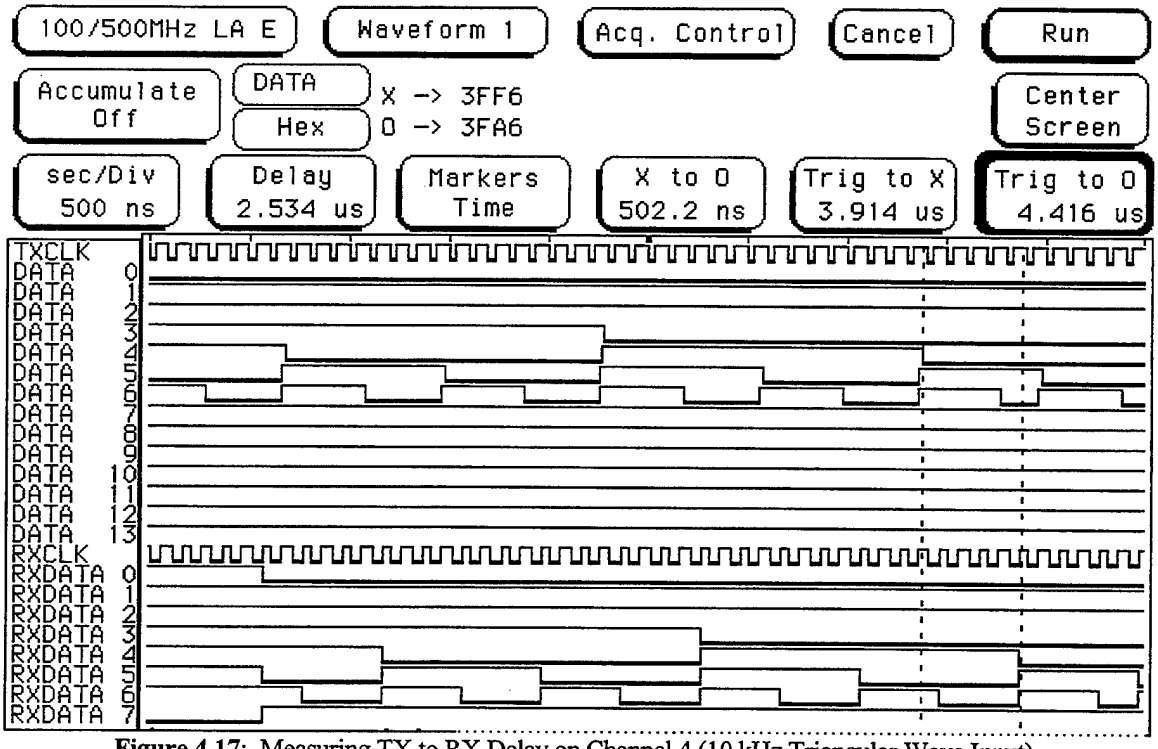


Figure 4.17: Measuring TX to RX Delay on Channel 4 (10 kHz Triangular Wave Input).

A 101.0 kHz triangular wave input was applied in the second test case. Here the transmitted binary patterns appear in Figure 4.18. Received binary patterns are found in Figure 4.19. Again the transmitted data pattern appears on the receiver data lines after a small delay. Figures 4.20 illustrates the measured delay between transmitting and receiving the data. In the second test case, the measured latency is 472.2 ns.

Additional test cases were applied to the data link using input signal frequencies of 1.01 MHz, 2.06 MHz, and 10.10 MHz. Results of these test cases appear in Figures 4.21 through 4.29. Transmitted binary patterns are shown in the first logic analyzer figure for each test case. Received binary patterns are found in the subsequent figure of each test case. The last figure for each test case illustrates the measured latency. For these test cases, the measured latency is 472.2 ns or 482.2 ns. Occasional *glitches* (in HP logic analyzer terminology) may appear in transmitter data patterns. These glitches are caused by noise on the transmitter board data lines or aberrations in logic analyzer triggering. An example of a *glitch* is shown in Figure 4.21 at point ❶. These glitches are not actually transmitted as evident in observing the receiver data lines.

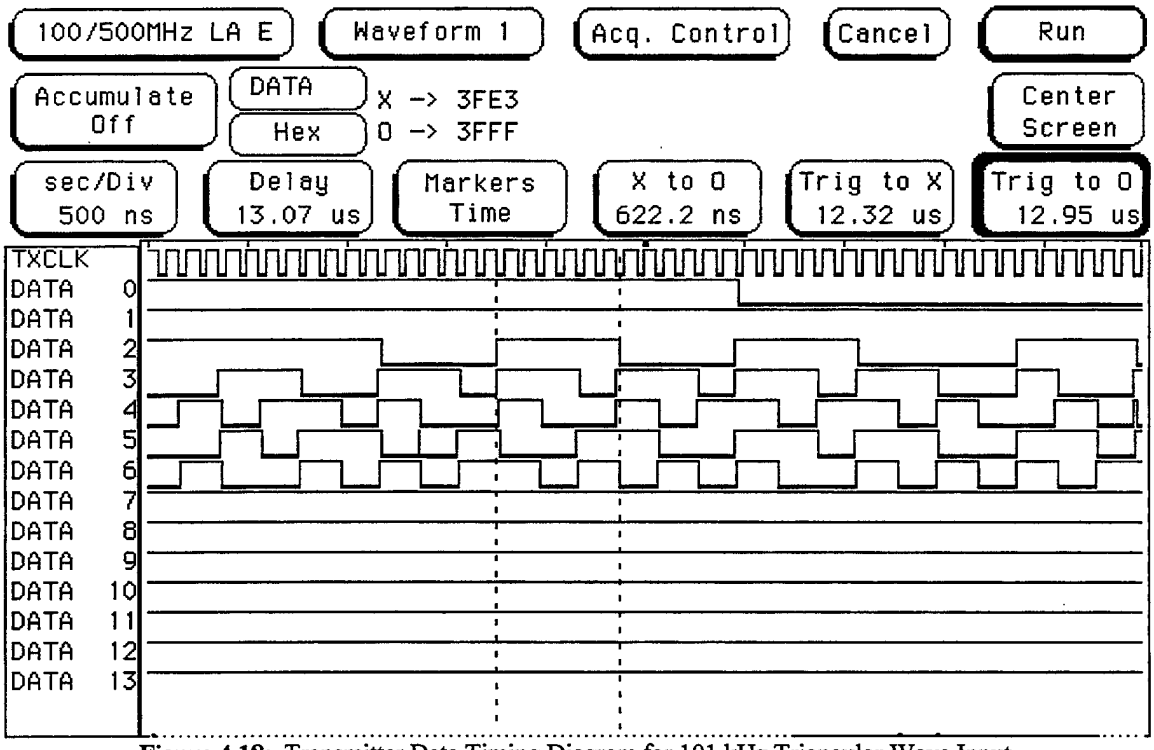


Figure 4.18: Transmitter Data Timing Diagram for 101 kHz Triangular Wave Input.

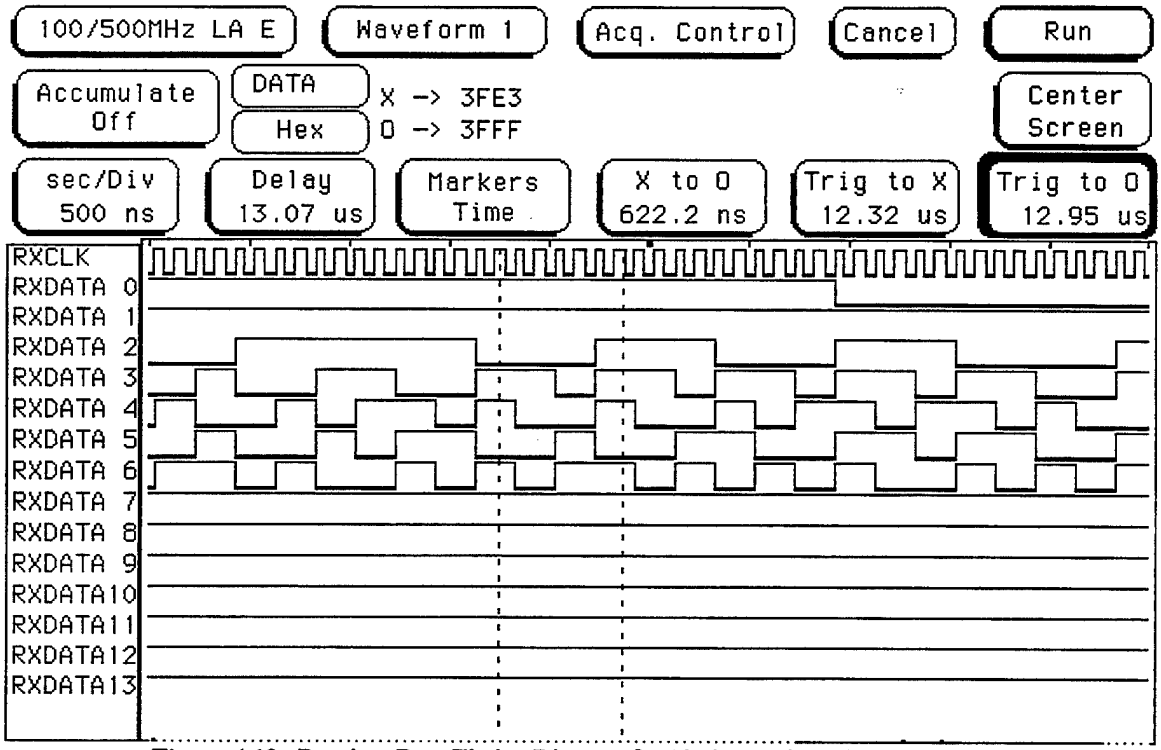


Figure 4.19: Receiver Data Timing Diagram for 101 kHz Triangular Wave Input.

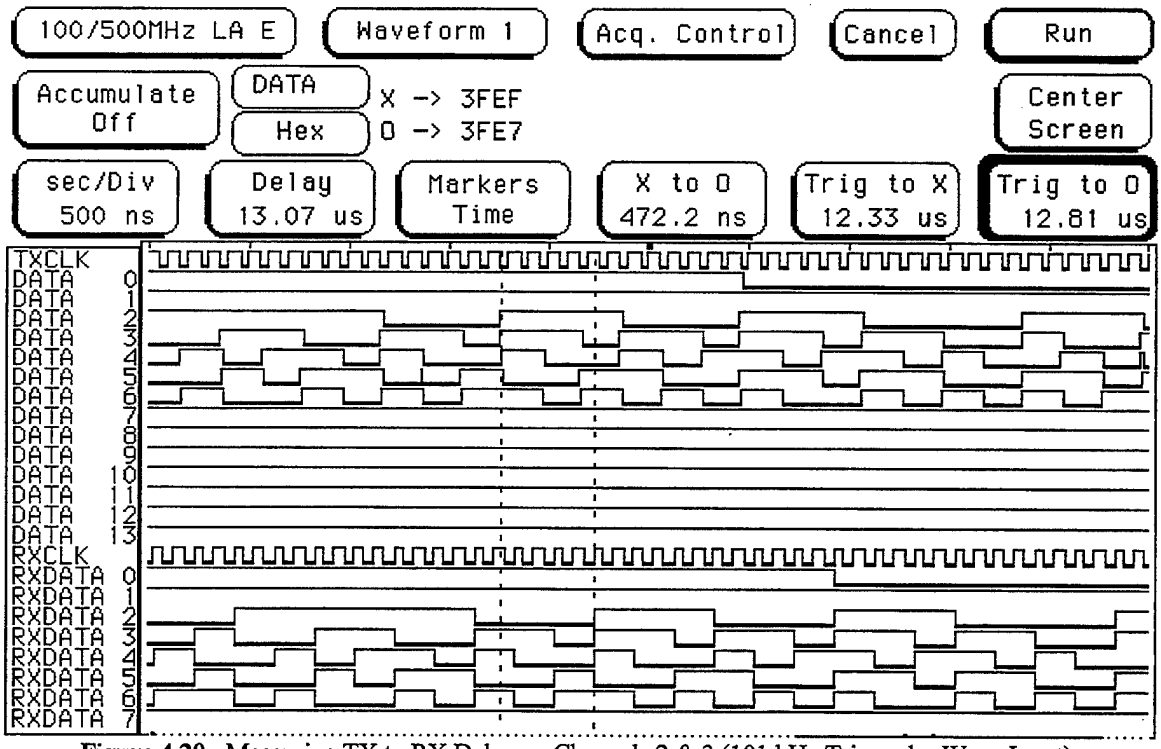


Figure 4.20: Measuring TX to RX Delay on Channels 2 & 3 (101 kHz Triangular Wave Input).

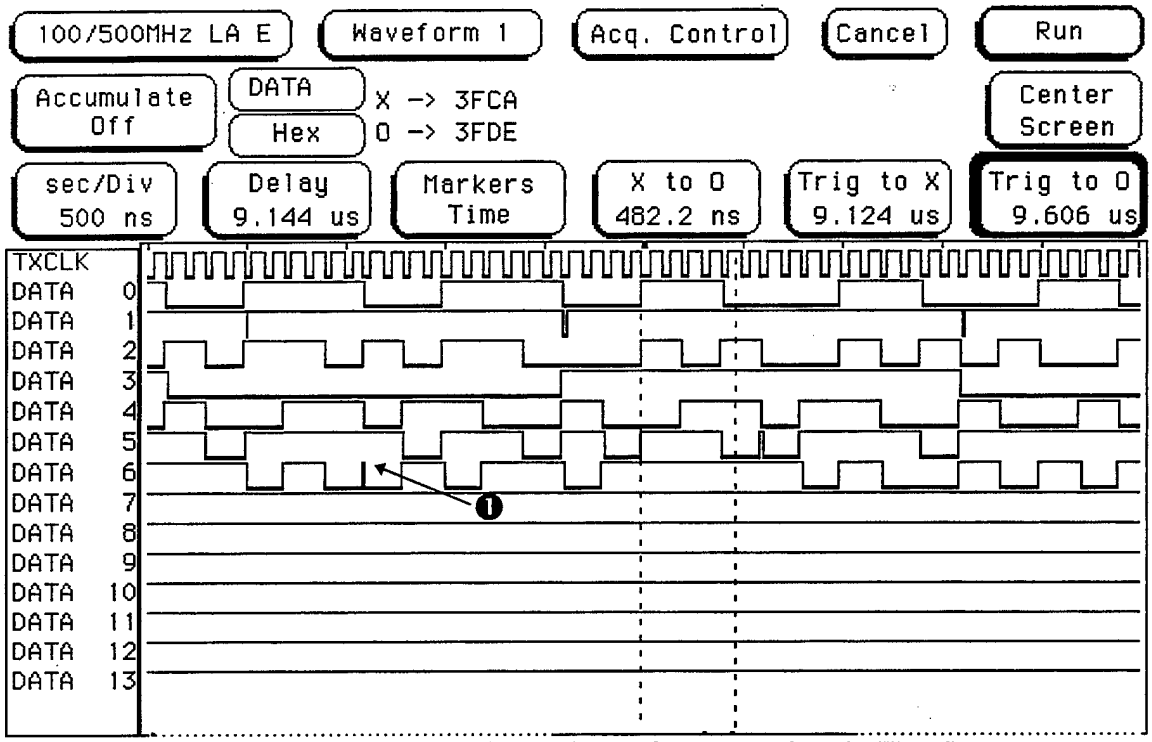


Figure 4.21: Transmitter Data Timing Diagram for 1 MHz Triangular Wave Input.

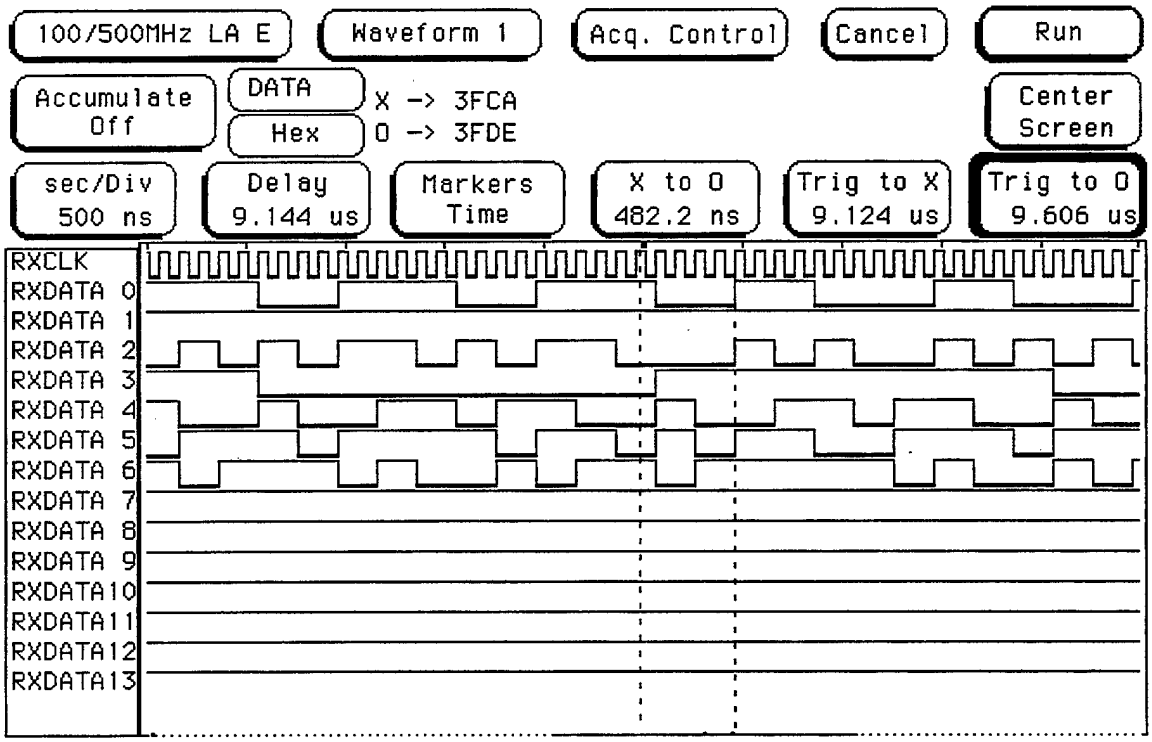


Figure 4.22: Receiver Data Timing Diagram for 1 MHz Triangular Wave Input.

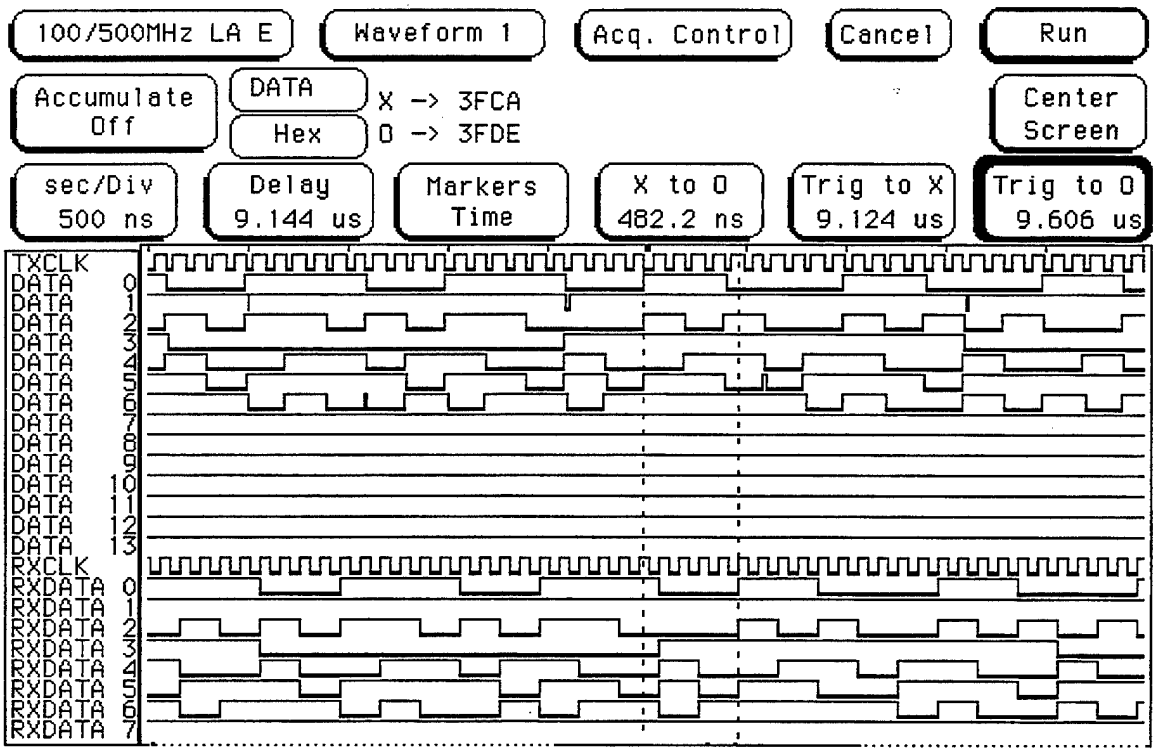


Figure 4.23: Measuring TX to RX Delay on Channels 0, 2, & 5 (1 MHz Triangular Wave Input).

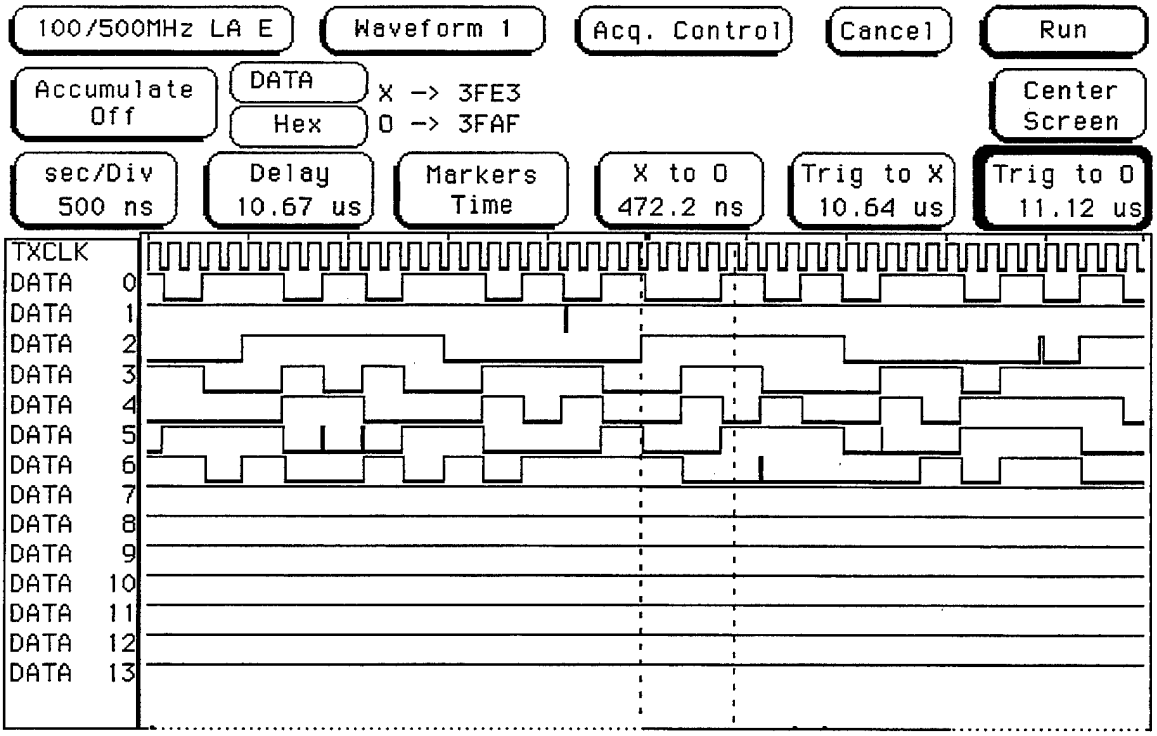


Figure 4.24: Transmitter Data Timing Diagram for 2 MHz Triangular Wave Input.

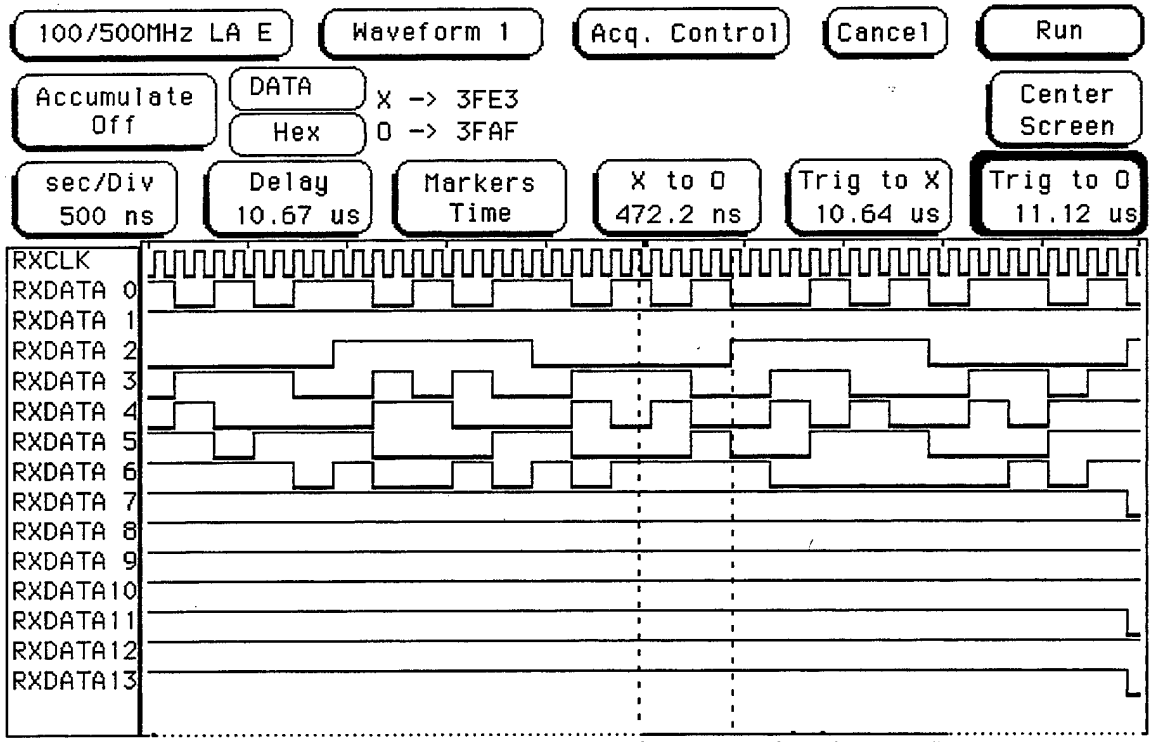


Figure 4.25: Receiver Data Timing Diagram for 2 MHz Triangular Wave Input.

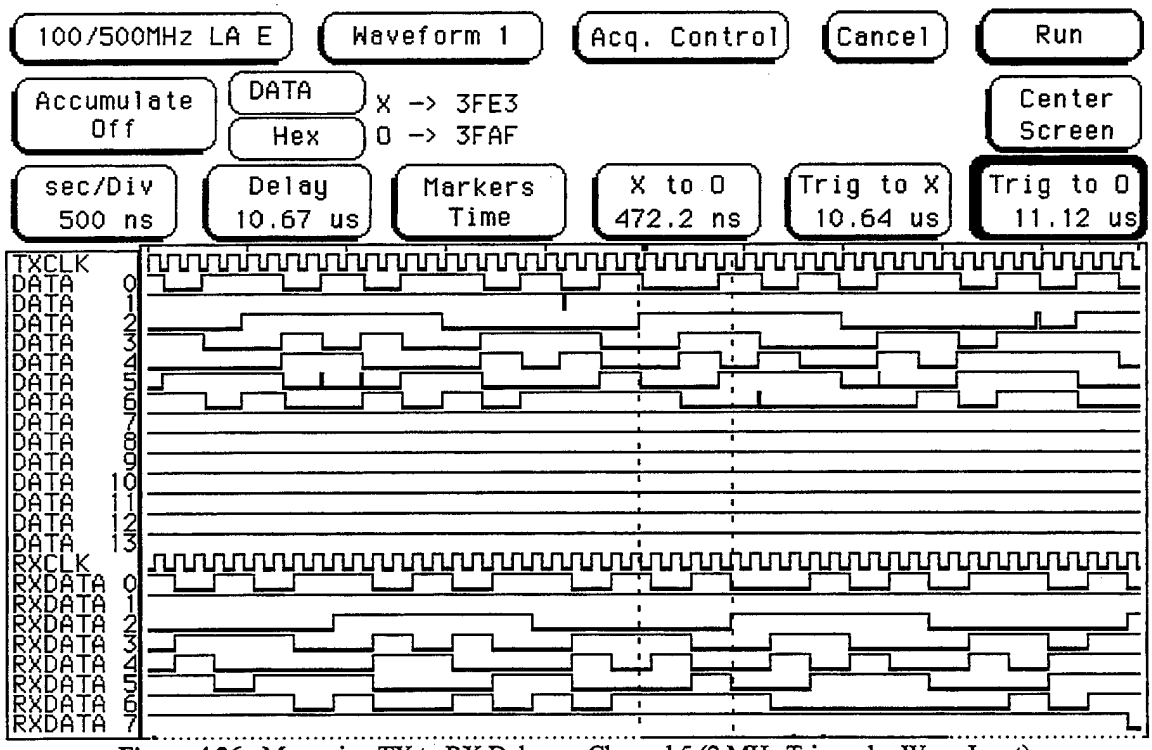


Figure 4.26: Measuring TX to RX Delay on Channel 5 (2 MHz Triangular Wave Input).

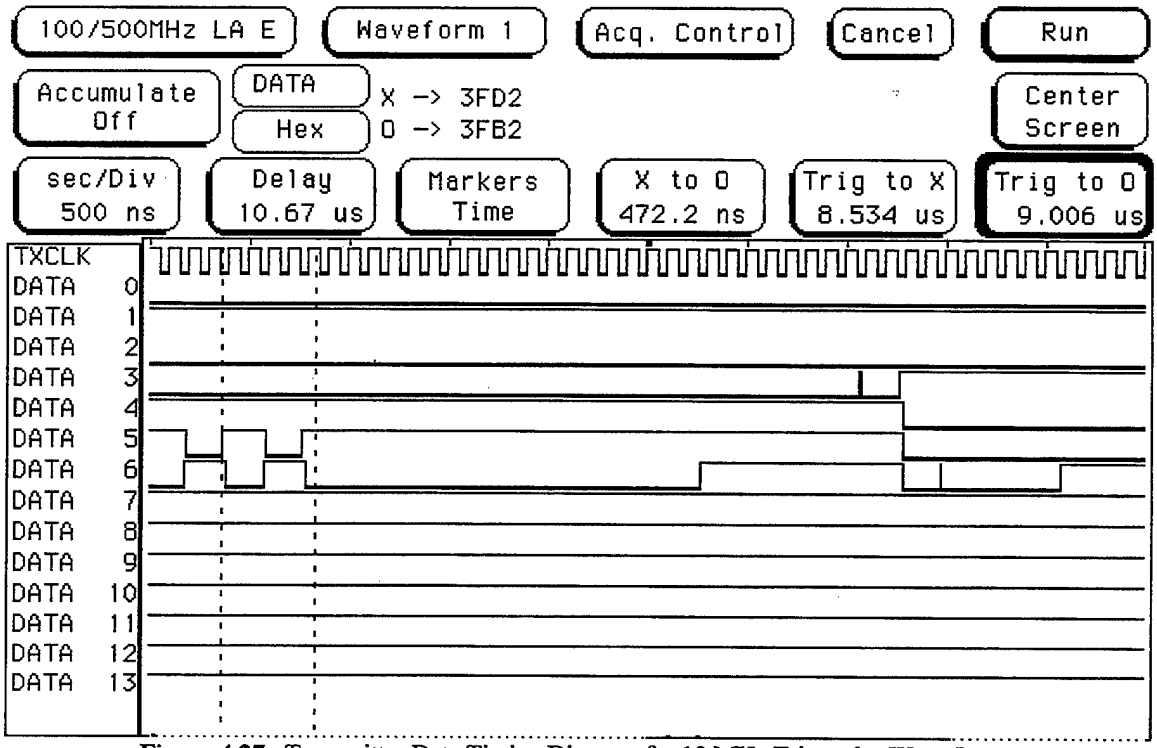


Figure 4.27: Transmitter Data Timing Diagram for 10 MHz Triangular Wave Input.

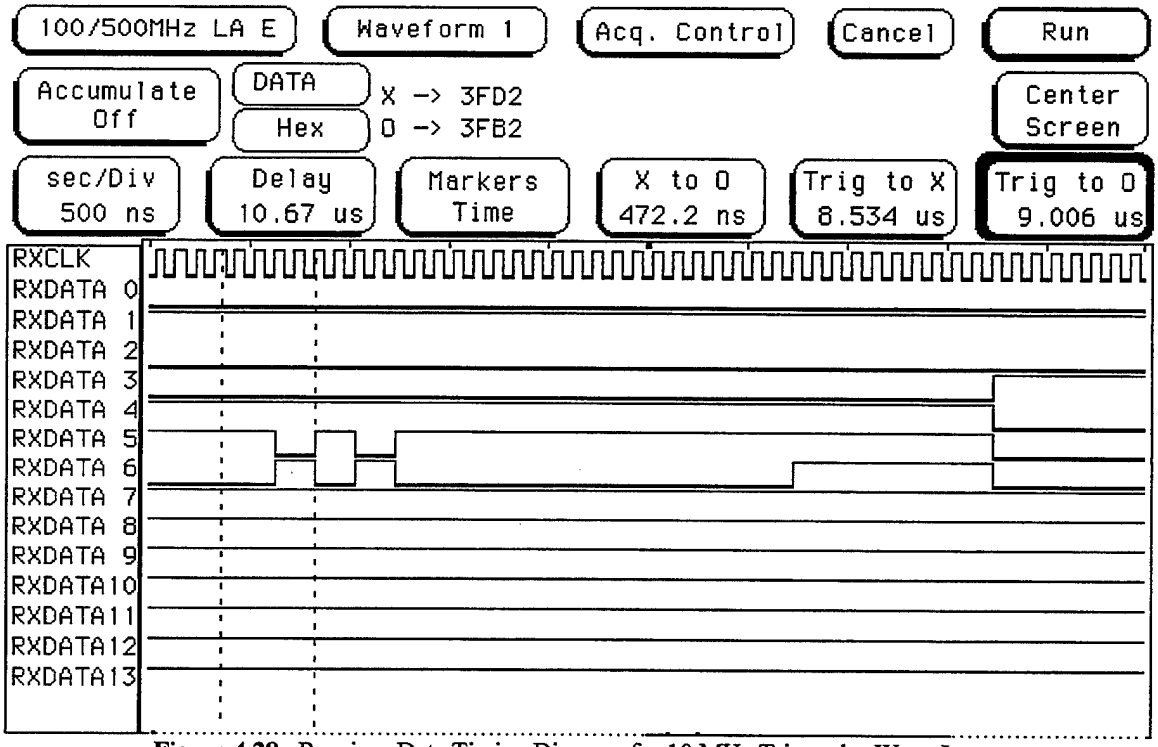


Figure 4.28: Receiver Data Timing Diagram for 10 MHz Triangular Wave Input.

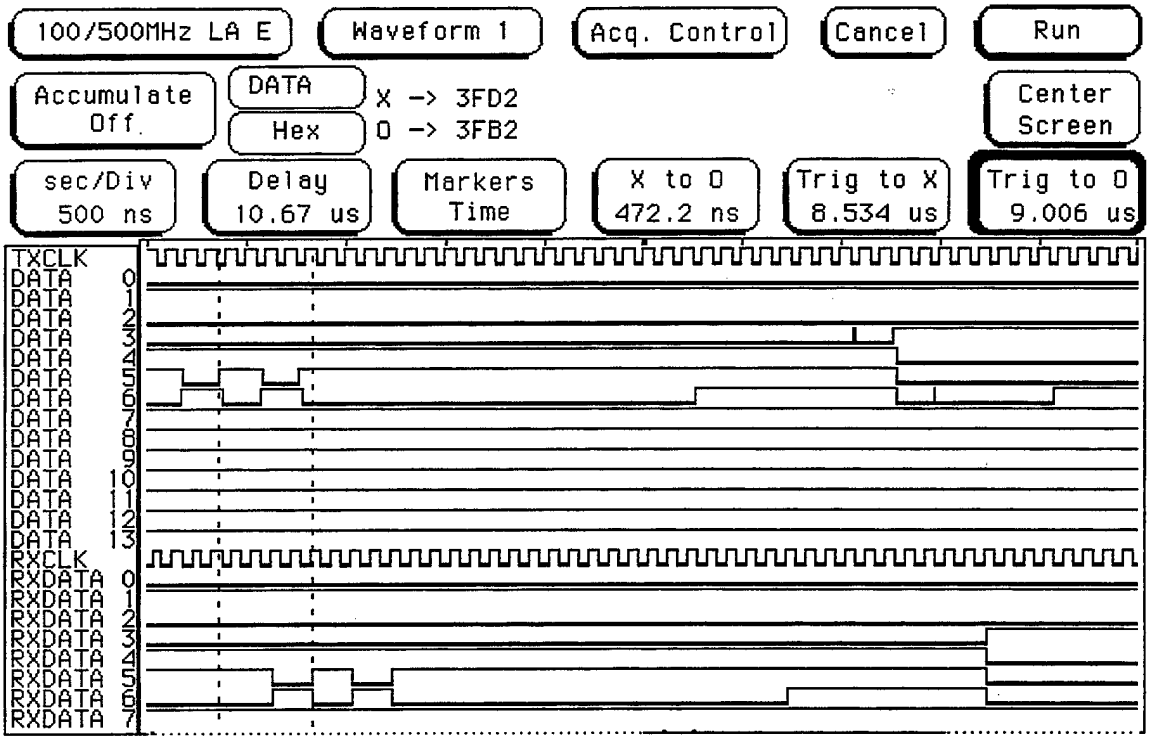


Figure 4.29: Measuring TX to RX Delay on Channel 5 (10 MHz Triangular Wave Input).

All variable voltage testing used a 5.5 m single-mode optical fiber link (with 1.56 dB of loss) with the exception of the data generated for Figure 4.30. A direct connection (meaning no intervening fiber link) was used to verify the measured latency is not affected by short fiber links. As Figure 4.29 shows, the latency between the transmitter and receiver was measured at 482.2 ns.

Measured transmitted and received serial data are shown in Figure 4.31. Again using the same eye pattern analysis used for the constant input, we see little noise and very little timing jitter in the serial data. T_b was again measured to be approximately 4.9 ns which equates to the 10.2 Mword/sec parallel rate for 20-bit frames. Refer to Figure 4.13 for a representative eye pattern diagram.

The results illustrated in Figures 4.14 through 4.30 demonstrate that the data link properly recovers the transmitted information. The link latency was approximately 482.2 ns +/– 20 ns (since each of the two logic analyzer markers is accurate to only 10 ns on the

displayed scale). Even under higher resolution (fewer seconds/division), link latency measurements were on average 482.2 ns.

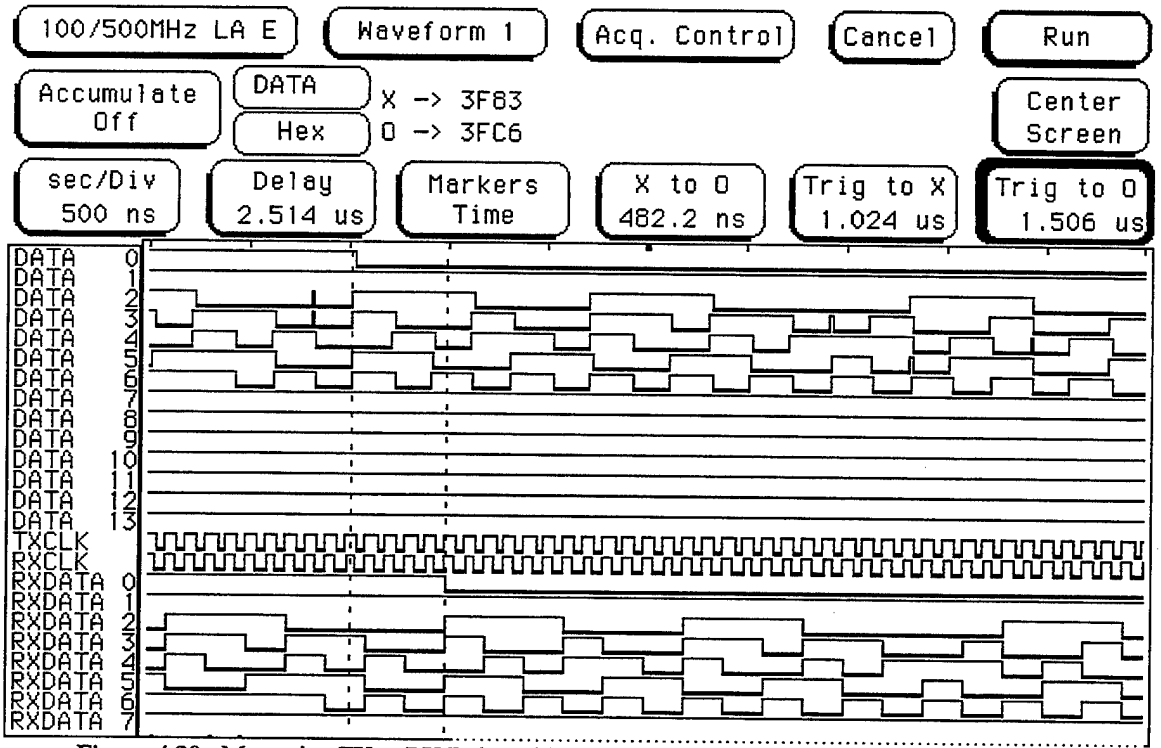


Figure 4.30: Measuring TX to RX Delay with No Fiber Link (101 kHz Triangular Wave Input).

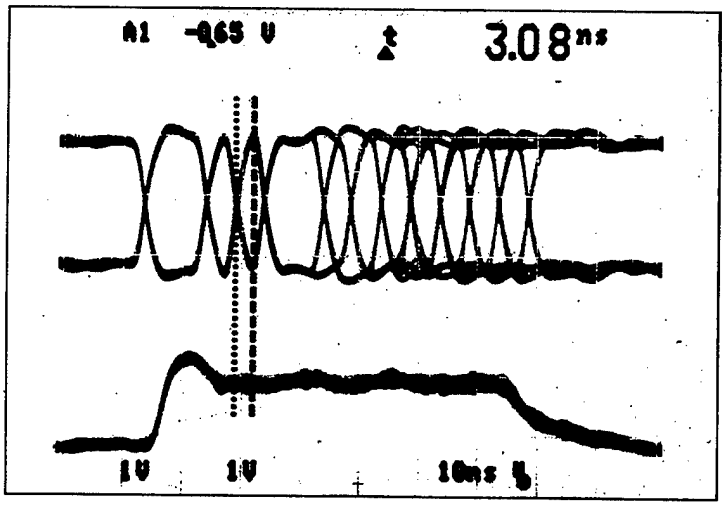


Figure 4.31: Eye Pattern Analysis of Transmitted Serial Data for Variable Input.

3. Pattern Generator Testing

The Hewlett-Packard logic analyzer is capable of generating specific test patterns for TTL data output. These patterns may be routed to the transmitter board in lieu of the ADC inputs signals via the 34-pin ribbon cable. Connections should be made on the data pins on the P1 bus on the transmitter board. The pattern generator available at the time of data link testing supports only eight channels. Full link testing with the pattern generator requires fourteen channels. This capability was unavailable during testing of the data link.

C. DESIGN PITFALLS AND CONCERNS

The seven least significant bits of the Datel ADS-944 ADC output do not follow the specified offset binary coding for the ADC (refer to Table A.4 in Appendix A for specific binary encoding patterns). Extreme analog inputs such as the negative full-scale voltage input (–1.25 Vdc) do work correctly. The ADS-944 (used for testing the data link) could not be calibrated accurately enough with available laboratory equipment. ADC calibration voltages require a high precision voltage (e.g., +76.3 μV) which could not accurately be measured by the lab equipment available for this research. Further, it is unlikely that the power supplies used in this research can maintain such a precise voltage. The calibration procedure is described in Reference 13. Due to the age of the ADC, it is also possible a component has failed on the ADS-944.

Structurally the transmitter and receiver control boards have a weak point at each J1 and J2 connection. The J1 and J2 connections are BLL ports using BCP's mini-coaxial cable (MMCX). The cable must be connected between an MMCX adapter on the fiber optic module and an MMCX adapter on the control board. Since the MMCX adapter has a surface mount design, there is difficulty in achieving a strong bond between the signal pad and the control board signal wire. This weakness can be corrected in a future PCB design.

The use of high-speed ECL devices in the data link control logic pose two possible pitfalls to the data link designer. The first is the large power consumption of ECL devices.

The second is adverse transmission line effects. Aside from providing power supplies capable of supplying sufficient current, the large power consumption of ECL will generate a great deal of heat. The designer must take into account thermal relief considerations such as heat sinks and air flow. Failure to do so will certainly shorten component life and reduce the reliability of the data link. Neglecting transmission line effects encountered in ECL will reduce signal noise margins and possibly cause signal loss. Matching the transmission line's characteristic impedance (when line length is greater than a few inches) is a must. Proper signal termination and series or parallel damping are essential to a good design. Signal noise and crosstalk may differ in on-site implementation so noise margins need to be as large as possible.

Buffer line logic (BLL) information is lacking at best in References 8 and 14. Improper BLL signal connections and terminations may degrade data link performance or even prevent proper operation. The BLL input signals must swing around digital ground. Logic high is +0.35 V and logic low is –0.35 V. BLL signals may be generated from ECL signals by using a DC-blocking capacitor (e.g., 0.1 μF). RX STRBIN is an ECL signal converted to BLL. Unused BLL outputs should be terminated with a 50 Ω resistor to ground.

BCP states the HP HDMP-101X chip set within the 15T/R modules are highly susceptible to electro-static discharge (ESD). The chip set has a voltage breakdown of approximately 50 volts compared to 2000 volts typical in most high-speed logic devices. Personnel may generate electro-static potentials in the range of 50,000 volts. By touching the device without protective ESD equipment (such as a grounding strap), a short-circuit between transistor inputs and outputs may occur (due to a buildup of charge which arcs through a dielectric to another surface with the opposite charge) [Reference 21: p. 108]. This effectively will destroy the chip set. Further, improper connection of the modules to components with a significant potential difference between ground planes may cause latch-

up in transistors. Therefore, the designer must abide by proper ESD workstation procedures when assembling components with the 15T/R. [Reference 8: p. 21]

The wire-wrapped prototype design proved the concept of the data link design. Signal quality may be improved with a printed circuit board design. Figure 4.32 compares signals without a ground plane against a design with signals over a ground plane (as in a PCB design). Note there is less ringing and noise on the signals. A PCB design was not developed due to time constraints.

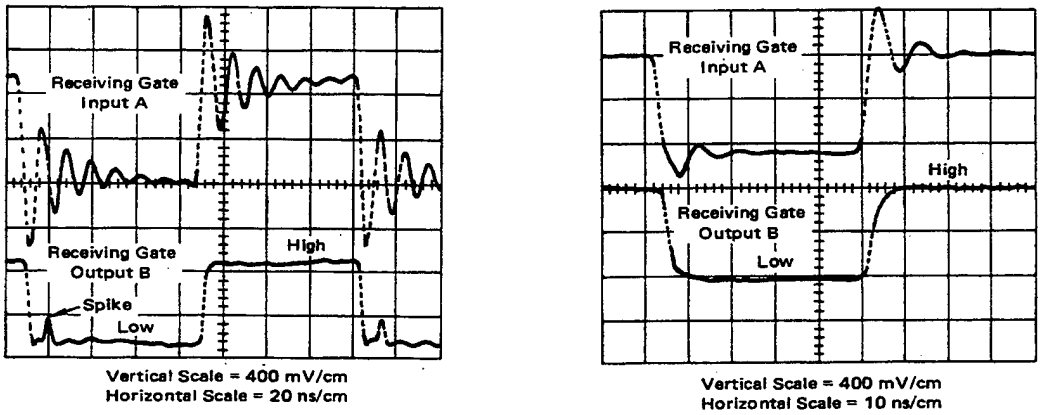


Figure 4.32: No Ground Plane Versus Ground Plane [Reference 19: p. 42]

This chapter illustrated that the prototype data link developed in this thesis operates correctly. The data link operated properly at the 200 Mbps serial data rate (140 Mbps effective). In Chapter V, the prototype data link is compared to a previous data link designed at the Naval Postgraduate School and compared to an optical data link designed by AT&T for military applications. Additionally, some data link improvements are suggested.

V. COMPARISONS AND DESIGN IMPROVEMENTS

This chapter compares the prototype data link developed in this thesis with two other data link designed for military applications. Suggestions for data link improvement are also made.

A. COMPARISONS WITH OTHER DATA LINKS

This section points out some similarities and differences with previously implemented optical data link designs used for military applications.

1. ECL and Electrical Transmission Media Data Link Design

In 1994, thesis research at the Naval Postgraduate School by Nejat Polat investigated designing a high-speed data link using a totally discrete ECL 10K design (see Reference 22). This earlier high-speed data link design for the high-resolution digital antenna system (referred to as the RF Receiver System in his thesis) attempted to transmit and receive 14 channels using a copper transmission medium vice optical fiber. The design utilized the same electronic sampling A/D converter used in this thesis to generate 14-bit parallel TTL level data. Following conversion from TTL to ECL logic levels, parallel data was serialized using an ECL-based parallel-to-serial design. The data words were transmitted at 5 Mwords/sec which produced a 70 Mbps serial data rate. The high speed serial data was connected to the receiver circuitry via copper wire which used a 70 MHz clock signal (generated on the transmitter board and connected to the receiver) to latch serial data. Synchronization between the transmitter and receiver was done through the use of a synchronization pulse (SYNC_PULSE) wire connecting the two circuits. With the use of an ECL serial-to-parallel conversion design in the receiver, the 14-bit binary words were recovered by the receiver. Testing of the data link did not achieve the goal of 5 Mwords/sec. A serial data rate of only 39 Mbps (or 2.786 Mwords/sec) was achieved. The 70 Mbps goal may not have been reached due to clock skew problems and neglecting ECL

transmission line effects. Connecting the transmitter and receiver with optical fiber was an eventual goal of the design, but this was never implemented. [Reference 22]

Other than the basic difference of transmission media, this earlier design differs from the present design in that only the serial data path (the optical fiber link) connects the transmitter and receiver. In the present design, there are no other connections between the TX and RX modules such as a CLOCK or SYNC_PULSE line. Clock recovery and link synchronization are recovered by the 15R receiver's PLL and internal VCO. Additionally, ECL logic is used only for basic functions such as logic conversion (TTL-ECL) and basic logical operations (NOR, OR, XOR). The entire parallel-serial conversion, serial-parallel conversion, clock generation, and clock recovery is carried out using the BCP TX and RX modules in conjunction with HP's HDMP-101X chip set. By using a design with only optical fiber connecting the TX and RX, low speed line delays and additional cable runs are eliminated. The earlier ECL electrical transmission media data link design is similar in theory to the Simplex I configuration of the HDMP-101X chip set.

The design of this thesis used the 5 Mword/sec data input and sampled it at a rate of 10 Mword/sec. Including the 4-bit frame control information and 16-bit data words, the current design achieved a serial data rate of 200 Mbps. However, only 14 bits of the 16 are used for the data word. Therefore, the effective serial data rate of the link is 140 Mbps. Potentially, the data link can achieve a serial data rate of 1.2 Gbps (16-bit mode at 60 Mword/sec). This equates to an effective serial data rate of 840 Mbps for 14-bit data words. For the 14-bit data word, a higher speed variant of the 15T/R modules will be required to achieve the 100 Mword/sec goal of the high-resolution digital antenna system.

2. Optical Data Link Design for Military Applications

The paper, "A High-Speed Surface-Mount Data Link for Military Applications" [Reference 23], describes an optical data link designed by AT&T in 1990. This section

details a comparison between the AT&T design and the thesis' high-speed data link. The benefit of this comparison is two-fold:

(1) the reader can gain an appreciation for optical data link technological advancements, and
(2) specific considerations for use in military applications may be addressed.

The AT&T design provides the same advantages of EMI immunity, increased security, weight and space savings, increased bandwidth, and good radiation tolerance. Their design used a 1310 nm LED vice a 1310 nm laser diode. Multimode fiber is common between both data links. The maximum serial data rate was 250 Mbps for the AT&T ODL® vice 1.2 Gbps for the high-speed, multi-channel data link of this thesis. At the present word rate of 10 Mword/sec, the thesis data link is operating at 200 Mbps.

The AT&T design is simply a point-to-point connection and does not incorporate circuitry for a specific type of transmission such as the time division multiplexing provided by the BCP TX/RX modules. The expected BER of the AT&T link is 10^{-9} while the thesis data link has an expected BER of 10^{-12}. The BER differences occur largely because the AT&T link uses an LED vice a laser diode, may only use multimode fiber, and relies on a lensed PIN photodiode. The Acarlar paper emphasizes that an optoelectronic data link must primarily be concerned with performance but also with the military environment. This means that packaging design, thermal stress analysis, and reliability estimation must be considered by data link designers. The AT&T design is meant for field use and may be power limited. The NPS design for shipboard use is not as power limited. [Reference 23]

B. DATA LINK DESIGN IMPROVEMENTS

The data link design described in this thesis is another step toward a reliable and cost-effective high-speed data link for shipboard use. Data link improvements must continue to be investigated and researched in order to provide the optimum data link subsystem for the high-resolution digital antenna system. Among the possible improvements are:

(1) developing a printed circuit board (PCB) design

(2) using higher performance ECL such as the 10H or ECLinPS families to improve noise immunities (requires PCB design)

(3) increasing the word rate to 60 Mword/sec

(4) develop a prototype mounting package for shipboard use

(5) explore thermal design improvements

(6) research other optoelectronic components to achieve 100 Mword/sec or greater

(7) develop a network interface to interface the data link with software

(8) develop a full-duplex link to support reception and transmission

Redundancy and other fault-tolerant concepts such as described in Reference 24 can provide a significant improvement to the reliability and availability of the data link. Several fiber optic module TX/RX pairs along with a fiber optic bundle can provide the redundancy. Other optical multi-channel communication system alternatives can also be explored, refer to Chapter 7 of *Fiber Optic Communications Systems* [Reference 25: pp. 272-319].

Following the comparison to the other data links mentioned in this chapter, Chapter VI discusses the description of the findings made during this research. Additionally, recommendations for further study are made to further the advances made during this research.

VI. CONCLUSION

Thus far the design, implementation, and testing of the multi-channel, high-speed, fiber-optic digital data link has been discussed. In this chapter, a description of findings and recommendations for further study are made. Following this chapter, several appendices with technical information required for the data link are included.

A. DESCRIPTION OF FINDINGS

Following design, implementation, and testing of the high-speed, multi-channel data link, it is clear that the prototype data link meets the required design goals. The prototype demonstrated that the simplex data link design of this thesis works and works effectively. The data link supports a fourteen channel TTL-compatible interface and supports a 10 Mword/sec parallel data word rate. The data link produces a 200 Mbps serial data rate of which 140 Mbps is the effective data rate. The observed data latency was 482.2 ns (+/– 20 ns). With minor modifications, the data link can support data words up to 17-bits at a parallel word rate of 60 Mword/sec (giving an effective serial data rate of 1.02 Gbps). Single-mode and multi-mode fiber links are supported by the data link.

The data link is a cost-effective solution for a point-to-point shipboard data link. Control logic to operate the fiber optic modules is relatively inexpensive. The total cost of each simplex link is in the range of only a few thousand dollars. Weight and space savings are also achieved by the data link when compared to existing electronic data link systems.

B. SUMMARY

The high-speed data link described in this thesis is only an interim step toward a reliable, dependable, and cost-effective data link for use with the high-resolution digital antenna system. While the digital antenna system is still in its infancy, the data link provides more than enough bandwidth for system testing and integration. The data link's resolution can easily be expanded up to 17 channels and even provide a six-fold increase in

data rate. (Only a five-fold increase in data rate can be achieved if the channel resolution is between 18-21.) Knowledge and experience learned in this data link research is beneficial in developing a robust high-resolution digital antenna system.

C. RECOMMENDATIONS FOR FURTHER STUDY

While the prototype design meets its design goals, there remain several improvements which may be made to the high-speed data link system. Among possible improvements are:

(1) Increasing the operating data rate of the prototype data link.

(2) Implementing a printed circuit board (PCB) design.

(3) Applying fault-tolerant concepts to the data link design.

(4) Developing TX and RX enclosures to allow field testing of the data link.

(5) Developing a full-duplex data link for comparison to a dual simplex data link.

(6) Examining alternative electro-optic designs to meet future digital antenna system requirements.

In the near term, data word resolution of the digital antenna system is likely to remain at 14-bits. Until the resolution increases, the prototype may be improved by increasing the data rate. Data rate may be increased by adjusting the 15T/R module operating range jumpers (see Table A.8 in Appendix A) and by replacing the TX and RX control board crystal oscillators with the frequency which matches the desired parallel word rate. 10K family ECL devices used in the prototype have a maximum operating frequency in the 100 to 150 MHz range. The maximum parallel word rate of the prototype requires 60 MHz crystals. Ideally the prototype will work as designed for the increased word rate. However, crosstalk among wiring and noise in the ground plane may interfere with signal noise margins and impair link operation. Therefore, it is recommended significant increases in data rate be made hand-in-hand with a PCB design.

The prototype design of the data link can be improved by making a printed circuit board (PCB) implementation of the design. PCB layout issues and electrical performance issues could be addressed. Such a design would reduce electrical interference and noise encountered in a wire-wrapped/soldered prototype board design. MECL 10H family devices may be used in a PCB design. The 10H family provides improved noise margins and higher switching speed. A PCB design coupled with MECL 10H devices are the best choices for operating the data link at its maximum data rate.

Improving the data link using fault-tolerant design methods could be examined in a more detailed fashion. Such a design would require the use of multiple G-Link module pairs and a optical fiber bundle. The pros and cons of developing a redundant design could be investigated. A fault-tolerant data link is essential for critical military applications. Reference 24 provides good coverage of fault-tolerant design issues.

In order to conduct field testing of the data link, mechanical enclosures for the TX and RX circuit boards must be developed. Developing enclosures requires studying thermal relief, packaging, and mechanical stress requirements. Further, miniature power supplies would be required to operate the data link. EMI shielding and EMC concerns could also be addressed in this study. This improvement project is ideal for a Power Systems student with an interest in digital design and electro-optic communications.

Most naval communications systems include an antenna system capable of reception and transmission. At some point, the digital antenna system should provide a transmission data link in addition to the reception data link designed in this thesis. One advantage of components such as the BCP 15T/R is that they may be configured in both simplex and full-duplex designs. The data link for a bi-directional antenna system could be implemented with two simplex links (as designed in this thesis) or in a full-duplex configuration. A study could be done to compare these two options. The full-duplex configuration should be the better option when using the 15T/R modules because local and remote loopback options

would be available. These loopback options enable the user to test operation of individual TX and RX modules and the optical fiber link.

Investigation into alternative technologies to the G-Link modules might be worthwhile. More advanced high-speed multiplexing transmitter/receiver sets such as the 15T/R modules should be available in the near future. The present envelope for the digital antenna system speed is 100 MHz. Electro-optic transmitter/receiver sets are being developed in the 2.5 Gbps range. Such devices should be able to accommodate the present digital antenna system performance envelope even with increased resolution. Optical TDM technologies are another possible alternative. Several articles in the bibliography may provide insight into optical TDM technologies.

APPENDIX A. COMPONENT SPECIFICATIONS AND DATA SHEETS.

The following is a brief summary of the components used in the data link design. More complete specifications may be found in the respective data books. Note that * denotes active low logic. Also, **D** and **B** denote data bits (e.g., D0..D13, B1..B14).

A. DATEL ADS-944 ANALOG-DIGITAL CONVERTER

The following is a brief summary of the component specifications for the Datel ADS-944 5 MHz, 14-bit Sampling A/D Converter.

ADC Features

- 14-bit resolution
- 5 MHz minimum sampling rate
- Edge-triggered
- 2.95 W power consumption
- Bipolar analog input range of +/- 1.25 V

Functional Diagram

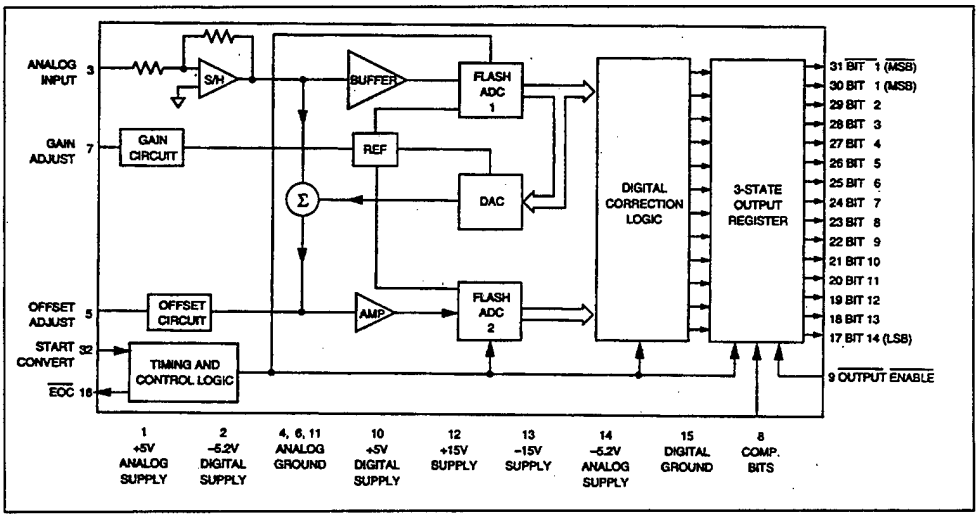


Figure A.1: ADS-944 Functional Diagram [From Reference 13: p.1-143].

Input-Ouput Connections

PIN	Function	PIN	Function
1	+5 V Analog Supply	32	START CONVERT signal
2	-5.2 V Digital Supply	31	B1* (MSB*)
3	Analog Signal Input (+/- 1.25 V)	30	B1 (MSB)
4	Analog Ground (Floating Ground)	29	B2
5	Offset Adjust	28	B3
6	Analog Ground (Floating Ground)	27	B4
7	Gain Adjust	26	B5
8	Complement Data Bits	25	B6
9	Output Enable * (OE*)	24	B7
10	+5 V Digital Supply	23	B8
11	Analog Ground (Floating Ground)	22	B9
12	+15 V Supply	21	B10
13	-15 V Supply	20	B11
14	-5.2 V Analog Supply	19	B12
15	Digital Ground (Chassis Ground)	18	B13
16	End Of Convert * (EOC*)	17	B14

Table A.1: ADS-944 I/O Connections [After Reference 13: p. 1-143].

ADS-944 Pin Connection Diagram

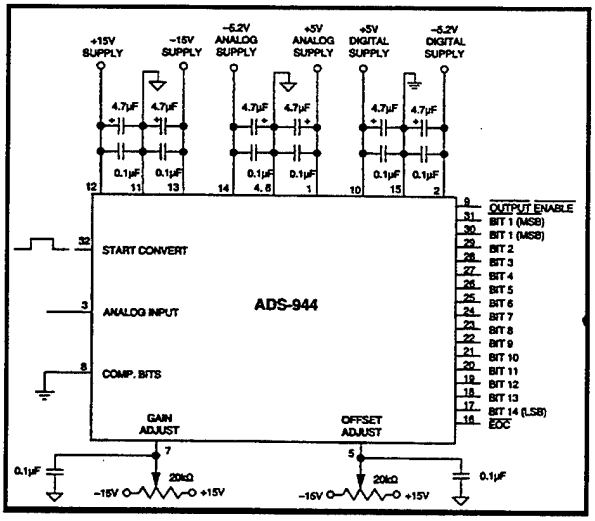


Figure A.2: ADS-944 Pin Out Diagram [From Reference 13: p. 1-146].

Ribbon Cable and Connector Connections

Two connection buses are used onboard the ADS-944 Evaluation Board. P2 is a 26-pin header which routes power and ground supplies to the ADC circuitry. P1 is a 34-pin header which routes control and data signal output for the ADC user. Note that 14 pins of P1 are connected to digital ground. This is used to reduce possible crosstalk and signal attenuation in the output ribbon cable.

Pin	Color	Function	Pin	Color	Function
1	Yellow	D1*	2	Orange	Output Enable*
3	Red	NC	4	Brown	Start Convert
5	Black	Complement	6	White	B14 (LSB)
7	Gray	Digital Ground	8	Violet	B13
9	Blue	Digital Ground	10	Green	B12
11	Yellow	Digital Ground	12	Orange	B11
13	Red	Digital Ground	14	Brown	B10
15	Black	Digital Ground	16	White	B9
17	Gray	Digital Ground	18	Violet	B8
19	Blue	Digital Ground	20	Green	B7
21	Yellow	Digital Ground	22	Orange	B6
23	Red	Digital Ground	24	Brown	B5
25	Black	Digital Ground	26	White	B4
27	Gray	Digital Ground	28	Violet	B3
29	Blue	Digital Ground	30	Green	B2
31	Yellow	Digital Ground	32	Orange	B1 (MSB)
33	Red	Digital Ground	34	Brown	B1* (MSB*)

Table A.2: P1 Bus Connections.

Pin	Color	Function	Pin	Color	Function
26	Brown	Analog Ground	25	Red	Analog Ground
24	Orange	Analog Ground	23	Yellow	-5V Digital
22	Green	Analog Ground	21	Blue	-5V Digital
20	Violet	Analog Ground	19	Gray	+5V Digital
18	White	Analog Ground	17	Black	+5V Digital
16	Brown	Analog Ground	15	Red	-5V Analog
14	Orange	Analog Ground	13	Yellow	-5V Analog
12	Green	Digital Ground	11	Blue	-15V
10	Violet	Digital Ground	9	Gray	-15V
8	White	Digital Ground	7	Black	+15V
6	Brown	Digital Ground	5	Red	+15V
4	Orange	Digital Ground	3	Yellow	+5V Analog
2	Green	Digital Ground	1	Blue	+5V Analog

Table A.3: P2 Bus Connections.

ADC Output Coding Table

OUTPUT CODING			INPUT RANGE	BIPOLAR
MSB LSB	MSB LSB	MSB* LSB	+/- 1.25 V	SCALE
11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111	+1.249847	+FS -1 LSB
11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000	+0.937500	+3/4 FS
11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000	+0.625000	+1/2 FS
10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000	0.000000	0
01 0000 0000 0000	10 1111 1111 1111	11 0000 0000 0000	-0.625000	-1/2 FS
00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000	-0.937500	-3/4 FS
00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001	-1.249847	-FS +1 LSB
00 0000 0000 0000	11 1111 1111 1111	10 0000 0000 0000	-1.250000	-FS
OFFSET BINARY	COMPLEMENTARY OFFSET BINARY	TWO'S COMPLEMENT		

Table A.4: A/D 14-bit Binary Encoding [After Reference 13: p. 1-147].

ADC Timing Diagram

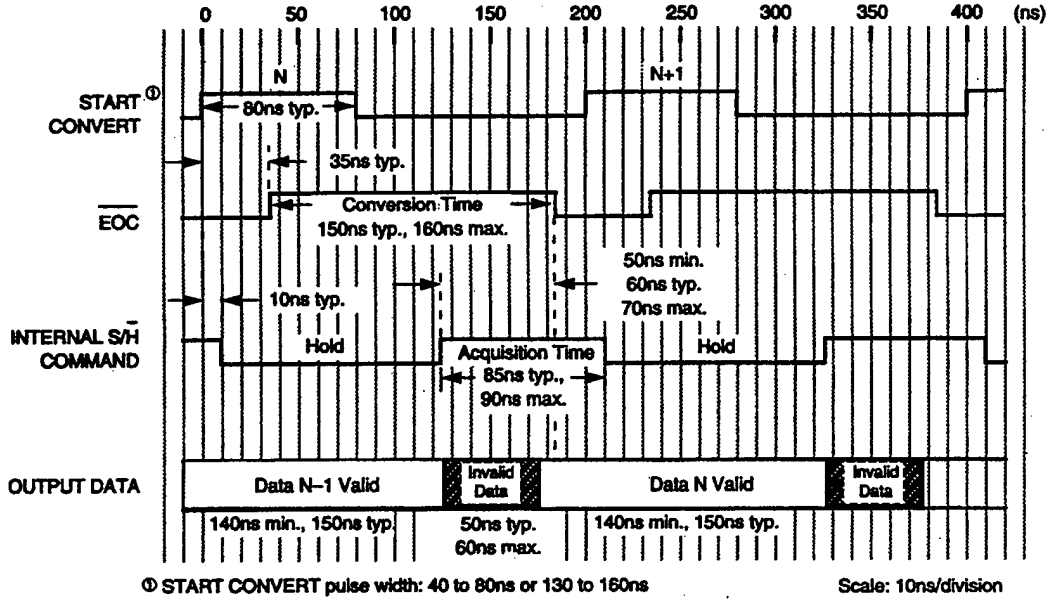


Figure A.3: ADC Timing Diagram [From Reference 13: p. 1-147].

ADS-944 Evaluation Board Schematic

Refer to Figure 2.13 in Chapter II.

B. BCP 15T G-LINK FIBER OPTIC TRANSMITTER

Model 15T Pin Function Table

Name	Pin	Type	Description
D0	34	I-ECL	Data Inputs. The first 16 data bits (D0..D15) are used with 16 bit mode. All are used with 20 bit mode. In the high-speed data link design, only the lower 14 data lines (D0..D13) are used.
D1	10		
D2	35		
D3	36		
D4	11		
D5	37		
D6	12		
D7	14		
D8	39		
D9	15		
D10	40		
D11	41		
D12	16		
D13	42		
D14	43		
D15	18		
D16	44		
D17	45		
D18	20		
D19	46		
RMTLB*	23	TTL	Remote Loopback.
FLAG	33	I-ECL	Flag bit. May be used as an extra data bit if FLAGSEL is active.
DAV*	30	I-ECL	Data Available. Tells the TX data is available on the data lines.
CAV*	6	I-ECL	Control Word Available. Tells the TX a control word is available on the data lines. Overrides DAV*.
RFD	8	O-ECL	Ready for data. Output which tells the user the G-Link is ready to transmit data.
STRBIN STRBIN*	17 19	I-H50	Data clock input. Used to tell the TX, the parallel word rate. STRBIN* is not used in this variant of the 15T module.
STRBOUT	7	O-ECL	Data clock output. Outputs the frame rate derived from the STRBIN clock.
LOOPEN	48	I-ECL	Loopback Control. If active, the LOUT serial data output is used vice the fiber link.
FLAGSEL	29	I-ECL	Flag bit mode select. Determines if the FLAG bit is used

			for data or if it is used as an extra error detection bit.
M20SEL	4	I-ECL	16/20 Mode Select. Determines whether 16-bit or 20-bit mode transmission is used.
MDFSEL	28	I-ECL	Double-Frame Mode Select. Allows transmission of a double word data path using only a single word interface.
DIV0 DIV1		Jumpers	VCO Divider Select. Determines the TX speed range.
RST*	47	I-ECL	Chip Reset. Resets the TX.
ED	32	I-ECL	Enable Data. Used in full-duplex configurations to control RFD.
FF	31	I-ECL	Fill Frame Select. Determines which type of fill frame is sent when data and control words are not sent. Fill frames are required to keep the TX and RX in synchronization.
EHCLKSEL	5	I-ECL	External Clock Enable. Allows the STRBIN clock signal to be used vice the internal VCO clock signal. Used in testing low jitter test signals.
NC	21		No connection
LOUT	J1	O-BLL	Local Loopback Data. When LOOPEN is asserted, serial data is output here.
RIN	J2	I-BLL	Remote Loopback Data. When RMTLB* is asserted, serial data is input here.
GND	2,13,24,27,38, 49	Source	Ground (0 Volts)
-5V	1,25,26,50	Source	-5 V power supply input.
+5V	3	Source	+5 V power supply input.
Locked	9	O-ECL	Loop In-Lock Indication.
INV	22	O-ECL	Invert Signal. Tells whether current frame is being sent inverted or non-inverted (to maintain the DC balance).

Table A.5: 15T Pin Functions [After Reference 8: pp. 12-14].

15T Mechanical Package Diagram

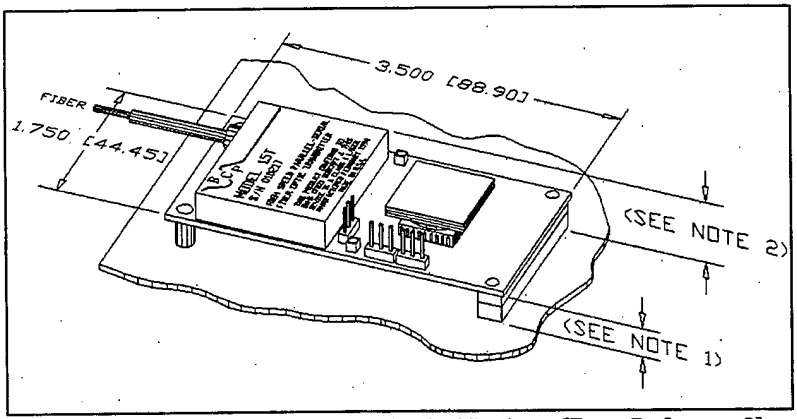


Figure A.4: 15T TX Module Mechanical Package [From Reference 8].

15T Module Specifications

- Compliant to SCI-FI Standard (ANSI/IEEE Standard 1596-1992)
- Uses HP G-Link encoding technology
- May be used in Serial-HIPPI implementations
- 16 or 20 bit parallel data modes
- Operates with single mode or multi-mode fiber
- Fiber link distances may be up to 1 km for multi-mode and 10 km for single mode
- 1310 nm or 1550 nm laser diodes available
- Parallel word rates: 7.5-60 Mwords/sec (16-bit mode) and 6.3-50 Mwords/sec (20-bit mode)
- Compatible with ECL technology
- Serial baud rate ranges between 150-1200 Mbaud

Operating Rates Table

Mode	DIV 1	DIV 0	Parallel Word Rate (Mword/sec)	Serial Data Rate (Mbps)
16-bit	0	0	42-60	672-960
	0	1	21-51	336-816
	1	0	11-25	176-400
	1	1	7.5-13	120-208
20 bit	0	0	35-50	633-1000
	0	1	18-42	360-840
	1	0	9-21	180-420
	1	1	6.3-10.5	125-210

Table A.6: 15T/R Operating Rates [After Reference 8: p. 8].

15T Timing Diagram

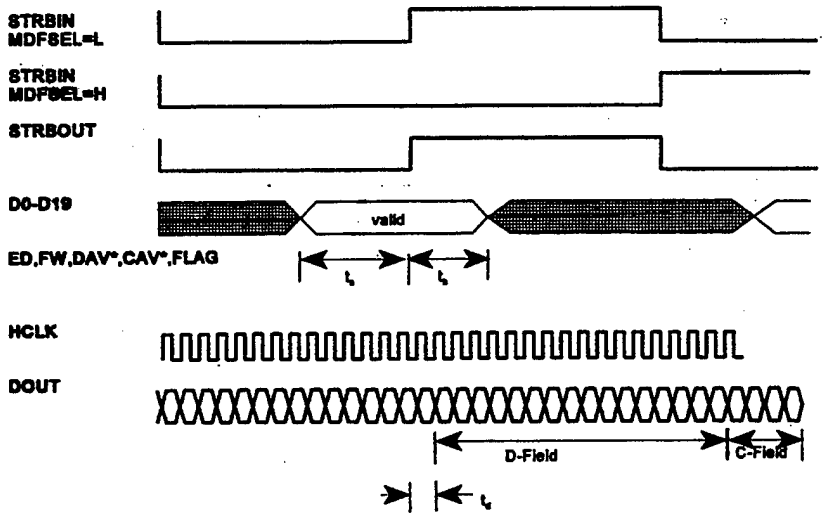


Figure A.5: 15T TX Timing Diagram [From Reference 8: p. 18].

C. BCP 15R G-LINK FIBER OPTIC RECEIVER

Model 15R Pin Function Table

Name	Pin	Type	Description
D0	29	O-ECL	Data Outputs. The first 16 data bits (D0..D15) are used with 16 bit mode. All are used with 20 bit mode. In the high-speed data link design, only the lower 14 data lines (D0..D13) are used.
D1	30		
D2	6		
D3	31		
D4	32		
D5	8		
D6	33		
D7	34		
D8	10		
D9	35		
D10	36		
D11	11		
D12	37		
D13	12		
D14	14		
D15	39		
D16	15		
D17	40		
D18	41		

D19	16		
LOOPEN	7	I-ECL	Local Loopback Control. Determines whether LIN (J1) is used for serial input or if the optical fiber link is.
FLAG	42	O-ECL	Flag bit. May be used as an extra data bit if FLAGSEL is active.
LINKRDY*	20	O-ECL	Link Ready Indicator.
DAV*	45	O-ECL	Data Available. Data is available for output.
CAV*	44	O-ECL	Control Word Available.
STRBOUT	46	O-ECL	Data clock output. PLL recovered data clock output.
FLAGSEL	47	I-ECL	Flag bit mode select. Determines if the FLAG bit is used for data or if it is used as an extra error detection bit.
M20SEL	47	I-ECL	16/20 Mode Select. Determines whether 16-bit or 20-bit mode transmission is used.
DIV0 DIV1		Jumpers	VCO Divider Select. Determines the TX speed range.
FDIS	9	I-ECL	Frequency Detector Disable Input. When asserted, disables the RX PLL frequency detector and enables the phase detector.
ACTIVE	17	I-ECL	Chip enable.
SMRST0* SMRST1*	23 48	I-ECL	State Machine Status Inputs. Normally, SMRST0* is used as a reset signal.
STAT0 STAT1	21 19	O-ECL	State Machine Status Outputs.
FCLK	4	O-ECL	Frame Clock Monitor.
FF	18	O-ECL	Fill Frame Status. Determines if the current frame is a fill frame or not.
ERROR	43	O-ECL	Received Data Error. Asserted when an invalid frame is received. In other words, the received frame is not a data frame, a control frame, or a fill frame.
RXALM*	5	Open Collector	Receiver Alarm. Indicates receiver failure or low optical input power.
LIN	J1	I-BLL	Local Loopback Data. When LOOPEN is asserted, serial data is input here.
ROUT	J2	O-BLL	Remote Loopback Data. When RMTLB* is asserted, serial data is output here.
GND	2,13,24,27,38, 49	Source	Ground (0 Volts)
-5V	1,25,26,50	Source	-5 V power supply input.
+5V	3	Source	+5 V power supply input.

Table A.7: 15R Pin Functions [After Reference 8: pp. 15-17].

15R Mechanical Package Diagram

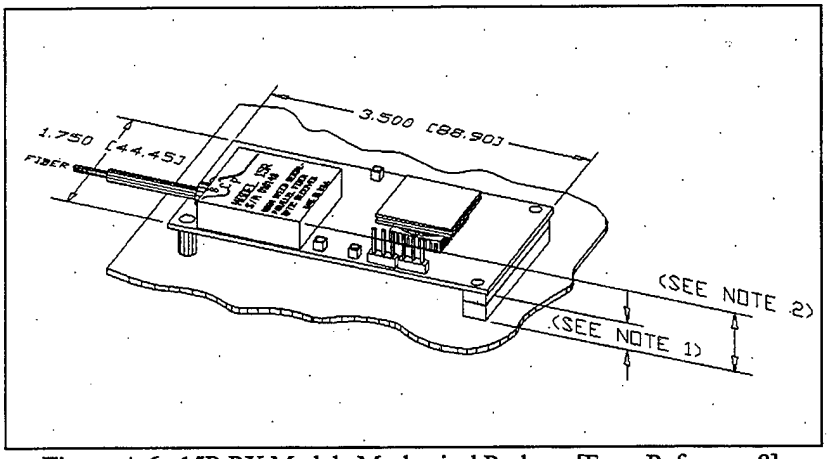
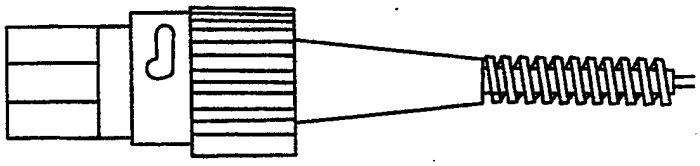


Figure A.6: 15R RX Module Mechanical Package [From Reference 8].

15R Module Specifications Table

- Compliant to SCI-FI Standard (ANSI/IEEE Standard 1596-1992)
- Uses HP G-Link encoding technology
- May be used in Serial-HIPPI implementations
- 16 or 20 bit parallel data modes
- Operates with single mode or multimode fiber
- Fiber link distances may be up to 1 km for multimode and 10 km for single mode
- 1310 nm or 1550 nm laser diodes available
- Parallel word rates: 7.5-60 Mwords/sec (16-bit mode) and 6.3-50 Mwords/sec (20-bit mode)
- Compatible with ECL technology
- Serial baud rate ranges between 150-1200 Mbaud

ST Fiber Connector Used for Optical Link



15R Timing Diagram

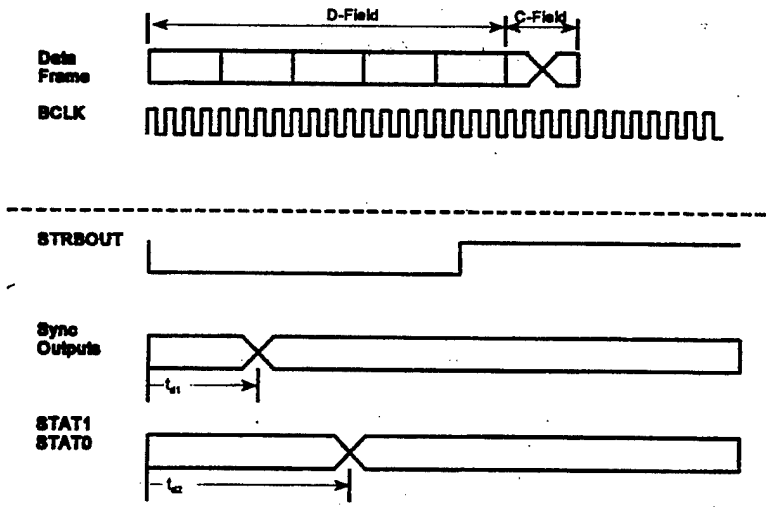


Figure A.7: 15R RX Timing Diagram [From Reference 8: p. 19].

D. HEWLETT-PACKARD HDMP G-LINK CHIP SET

Typical Operating Rates Table

Mode	DIV 1	DIV 0	Parallel Word Rate (Mword/sec)	Serial Data Rate (Mbps)
16-bit	0	0	42-75	672-1200
	0	1	21-51	336-808
	1	0	11-25	168-404
	1	1	7.5-13	120-202
20 bit	0	0	35-62.5	700-1250
	0	1	18-42	350-842
	1	0	9-21	175-421
	1	1	6.3-10.5	125-211

Table A.8: HDMP-1012 & HDMP-1014 Typical Operating Rates [After Reference 14: p. 5].

HDMP-101X Timing Characteristics

Module	Parameter	Value (ns)
HDMP-1012 TX	**Setup Time.** Rising edge of STRBIN relative to D0-D19, ED, FF, DAV*, CAV* and FLAG	6.0 (minimum)
	Hold Time. Rising edge of STRBIN relative to D0-D19, ED, FF, DAV*, CAV* and FLAG	0.0 (minimum)
	STRBOUT - STRBIN delay.	1.5 (typical) 3.0 (maximum)
HDMP-1014 RX	**Synchronous Output Delay.**	2.0 (typical)
	State Machine Output Delay.	4.0 (typical)

Table A.9: HDMP-1012 & HDMP-1014 Timing Characteristics [After Reference 14: pp. 10-11].

TX-RX Typical Lock-Up Times

DIV 1	DIV 0	HDMP-1012 TX (msec)	HDMP-1014 RX (msec)	Zero Length Link (msec)
0	0	2.0	2.2	2.5
0	1	3.0	3.2	3.5
1	0	4.5	4.7	5.0
1	1	8.0	11.0	12.0

Table A.10: HDMP-1012 & HDMP-1014 Typical Lock-Up Times [After Reference 14: p. 12].

E. TTL FAMILY DATA SHEETS

Data sheets for the transistor-transistor logic (TTL) devices used in this thesis are found in common TTL data books. A table pin-out for TTL-compatible crystal oscillator is included since it is not typically not found in TTL data books.

TTL Crystal Oscillator

The crystal oscillators used in the data link are TTL-compatible. The oscillating signals generated are then used as clocking signals (following conversion to ECL). Table A.11 describes the pin-out for the TTL crystal oscillators.

Pin	Function
1	No Connection
7	GND
8	Output
14	V_{CC}

Table A.11: Crystal Oscillator Pin-Out.

F. ECL FAMILY DATA SHEETS

ECL data sheets and technical information is found in Reference 18. In ECL design, V_{CC} refers to the most positive voltage which is normally 0 Vdc (except for TTL-ECL translators where V_{CC} = +5.0 Vdc). GND refers to digital ground (typically 0 Vdc). V_{EE} is the most negative voltage which is normally –5.2 Vdc. V_{TT} is the pull-down voltage reference which is normally –2.0 Vdc. V_{BB} refers to the bias voltage which was not used in any logic devices in the data link design. Generally, input and output lines use a pull-down resistor of 100 Ω to V_{TT}. Other values may be required when interfacing with between ECL families.

APPENDIX B. SURVEY OF DIGITAL DESIGN CONSIDERATIONS.

A. ADC DESIGN METHODS AND TECHNIQUES

The Datel A/D converter used in this design uses TTL logic connections and a multi-pass flash A/D conversion architecture with digital correction logic [Reference 13]. Newer ADCs use a pipelined architecture to achieve high speed A/D conversion [Reference 12]. The ADC used in this data link design is a cost effective device for testing the operation of the data link.

1. START_CONVERT Options

Use of the ADC is straightforward when general TTL logic methods are known by the digital designer. A/D conversion can be controlled with an external START_CONVERT signal. A conventional TTL oscillator is used to generate the high frequency signal. Divide logic (such as the 74163) to divide the clock signal may be used. The appropriate clock signal is then fed through an non-re-triggerable monostable multivibrator (such as the 74121) to achieve the necessary pulse width of the START_CONVERT signal (40-80 ns or 130-160 ns). Pulse width is controlled by the formula $t_w(out) = C_{ext} * R_t * \ln(2)$. To improve the quality of the signal, a custom high speed voltage comparator may be used to alternate the clock signal between the rail voltages of 0 V and +5 V. Conventional voltage comparators such as the LM311 and LM710 do not have fast enough switching for use in an external START_CONVERT circuit.

2. Other ADC Design Concerns

As a reminder, the designer must verify that power supply connections through the ribbon cables (P2 bus) are not short circuited with the separating ground wires in the cable. The separation of supplies and control signals by ground wires is used to minimize crosstalk and maximize the length in which the cables may be run. V_{CC} and V_{EE} connections should also be filtered with decoupling capacitors to ground. A 0.01 μF capacitor is a good choice for individual chip supply filtering. For power supply buses, 0.1 μF polarized capacitors are

recommended. Monolithic capacitors were used in parts of the design with no observable adverse effects.

B. G-LINK DESIGN METHODS AND TECHNIQUES

The G-Link fiber optic TX/RX modules incorporate TTL, BLL, ECL, and optoelectronic technologies. Most signals used with these modules are a modified implementation of conventional ECL. The digital designer working with these modules must be familiar with general logic design, TTL and ECL components, and basic fiber optic principles. BLL is used only on a couple of connections and the description provided by the BCP Data Notebook [Reference 8] is sufficient.

1. General G-Link Design Concerns

Of note, the 15T/R fiber optic modules are *highly* susceptible to electro-static discharge (ESD) unlike most ECL devices which are reasonably resistant to ESD. The importance of using proper ESD prevention and grounding procedures cannot be over emphasized.

With the use of internal pull-down resistors, the 15T/R modules allow I-ECL *no connects* to default to ECL lows and ground connections to default to ECL highs. External to the 15T/R modules, the use of 300 Ohm pull-down resistors to V_{TT} produces true ECL pull-down values.

Undesirable noise is unavoidable in the prototype boards used with the 15T/R. Ideally, connections should be very short (less than two inches). A printed circuit board (PCB) design with a reliable ground plane should be used in follow-on designs. The small physical size of the fiber optic module pin packages and the nature of the prototype board designs provide numerous physical wiring challenges. Good soldering skills and understanding of PCB design rules are a must. Figure B.1 details the suggested circuit board layers for a good MECL PCB design. Of course, the number of layers and specific

design rules in a realized design will depend upon the available process. PCB design tools such as Protel's *Advanced PCB* include detailed information to assist the designer in proper PCB layout.

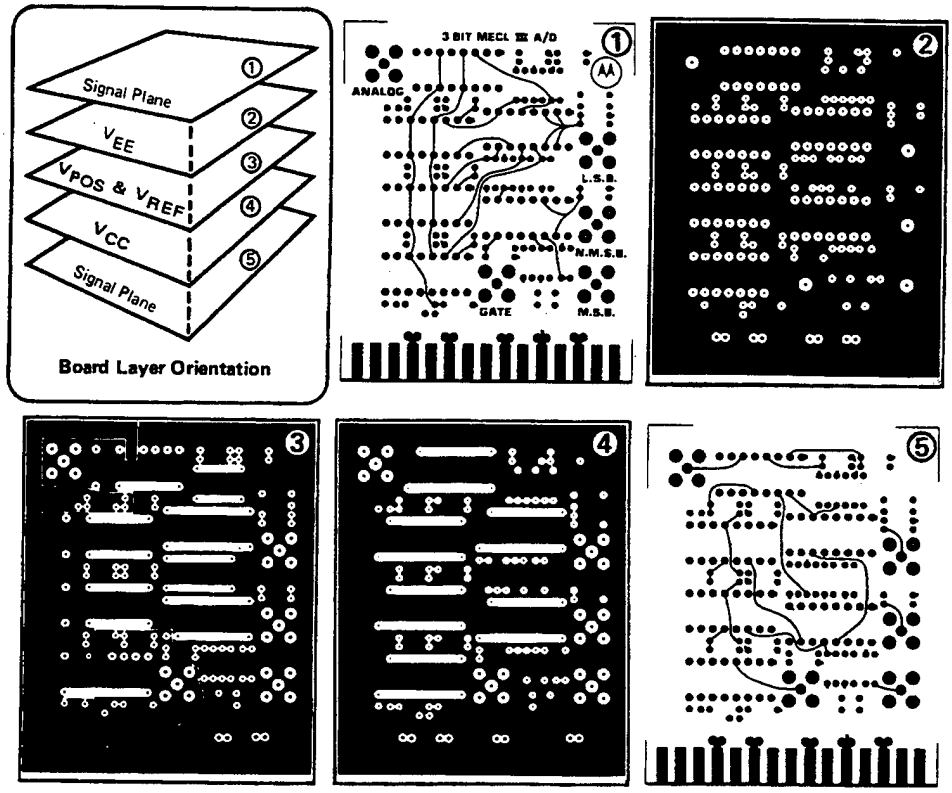


Figure B.1: MECL Printed Circuit Board Layers [Reference 19: p. 104].

C. TTL FAMILY DESIGN METHODS AND TECHNIQUES

Transistor-Transistor Logic (TTL) is the most common bipolar logic family. Once the dominant logic family, TTL has been supplanted by CMOS technology due to its lower power consumption, higher level of integration, and virtually unlimited fan-out [Reference 21]. TTL is still a factor in the discrete logic component market and provides a low-cost solution to many elementary logic design issues. TTL is unlikely to be used for more complex and high performance designs due to the advent of programmable logic devices

(PLD) and field programmable gate arrays (FPGA) technologies. However, it remains a de facto standard due to its widespread usage. [Reference 26]

In the data link design, TTL is mostly used for providing high frequency clock signals and for controlling the ADC. Most discrete logic design used the current-mode logic ECL family. For more details on using TTL in digital design, see Wakerly's text [Reference 21].

Consideration should be taken to use decoupling capacitors at all supply pins and on all supply buses whenever possible. Polarized capacitors are the best choice. However, monolithic capacitors do not display any adverse effects in this design. Capacitors in the range of 0.1 to 0.15 μF are ideal for supply bus decoupling and 0.01 μF are good for decoupling V_{CC} connections.

D. ECL FAMILY DESIGN METHODS AND TECHNIQUES

Emitter Coupled Logic (ECL) is a bipolar digital logic family which provides high performance by reducing logic swing (approximately 500 mV) and by operating at high current levels. With the high switching speed, the designer must be concerned with supply-induced noise and static power dissipation. The ECL family is not implemented with VLSI because of the static power dissipation problem [Reference 26]. However, it is used in modern supercomputing applications due to its high speed [Reference 21]. Two implementations of the ECL family are used in the data link design. The first devices are the Motorola MECL 10K family logic gates and the second are the 100K compatible ECL devices incorporated in the Hewlett-Packard HDMP chip set and the BCP 15T/R modules.

Motorola has been a leading innovator of modern ECL components. The Motorola ECL (MECL) family of 10K ECL integrated circuits are used in the data link implementation. The 10K family provides a high speed switching time of 1 ns, and the ability to use wire-wrap design techniques in prototyping systems with high speed logic.

Some highlights of the MECL family are: high speed, low cost, high fanout, very low noise generation, complementary logic outputs, low crosstalk, buffered outputs, and minimal degradation to temperature variations [Reference 19]. Higher performance ECL families such as the 100K, 10H, ECLinPS, and ECLinPS lite series are also available [Reference 20]. Specific design considerations are described in the Motorola MECL Data Book and in the Motorola MECL System Design Handbook (References 18 and 19, respectively). Included in this section is a brief description of the MECL and the 15T/R module ECL design considerations. For more specific details, the reader is referred to the MECL Data Book, the data sheets in Appendix A, and the Wakerly and Rabaey texts [References 21 and 26].

ECL logic is also central to the 15T/R fiber optic modules. The incorporated HDMP chip set utilizes 100K-compatible ECL devices to meet its high performance requirements. The BCP 15T/R modules also use ECL logic to drive the HDMP chip set and for other high performance requirements. Many of the design considerations are similar to the MECL family. However, there are some differences such as terminating ECL logic zeros to V_{TT} (with a 300 Ohm pull-down resistor) and no connections on the BCP modules defaulting to logic zeros (due to internal pull down resistors). Specific details on these components are found in the BCP 15T/R Data Book and in the data sheets included in Appendix A.

1. ECL Considerations for Data Link Components

The V_{EE} emitter voltage is tied to −5.2 V for both the MECL devices and for the 15T/R fiber optic modules. Decoupling capacitors (0.01 μF) are connected between each V_{EE} connection and ground to reduce the effects of noise in the power supply plane.

Several pins on the 15T and 15R modules are fixed at either an ECL logic zero or logic one to implement the Simplex III configuration. Logic ones are simply connections to ground. The fixed logic zero is a connection through a 300 Ohm resistor to V_{TT}. This termination to V_{TT} with the resistor, unlike standard ECL, will produce full ECL signal

amplitude [Reference 8]. Among the benefits of this connection method, is the increase in noise immunity of the signal.

The majority of MECL devices used in this design are TTL-MECL translators (MC10124) and MECL-TTL translators (MC10125). Several devices such as the A/D converter and crystal oscillators are TTL logic. The 15T/R fiber optic modules require mostly ECL inputs and provide ECL outputs.

2. An ECL Design Primer: The Basics

ECL design is often left out of digital design curricula. This section will assist the designer to become familiar with basic ECL design issues. An ideal ECL waveform appears in Figure B.2. High switching speed of ECL gates produces waveforms affected by transmission effects not often seen in TTL gates or low-speed CMOS devices. Observe that the ECL waveform has both an overshoot and an undershoot characteristic. Good ECL design maintains undershoot at less than 110 mV. Overshoot and undershoot are functions of line length, capacitive/induction loading, rise time, and other transmission line effects. These effects may be controlled by reducing system rise times (using a slower ECL family), reducing interconnect line lengths, and using matched, terminated transmission lines. All of these issues were considered in the data link design. [Reference 19: pp. 63-64]

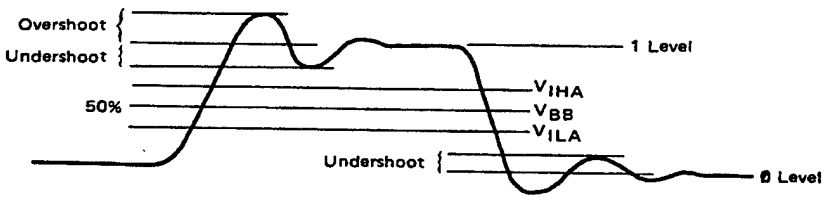


Figure B.2: Typical ECL Waveform [Reference 19: p. 64].

Unlike TTL, ECL has a very small voltage swing between high and low logic as illustrated in Figure B.3. Logic high is nominally at –0.9 V while logic low is nominally at –1.75 V. ECL maintains a constant current requirement as it steers current from one logic level to the other. Small noise margins are sufficient for ECL since very little power supply

or ground noise is generated (due in part to the common-mode signal rejection by the input structure's differential amplifier). [Reference 21: pp. 178-181]

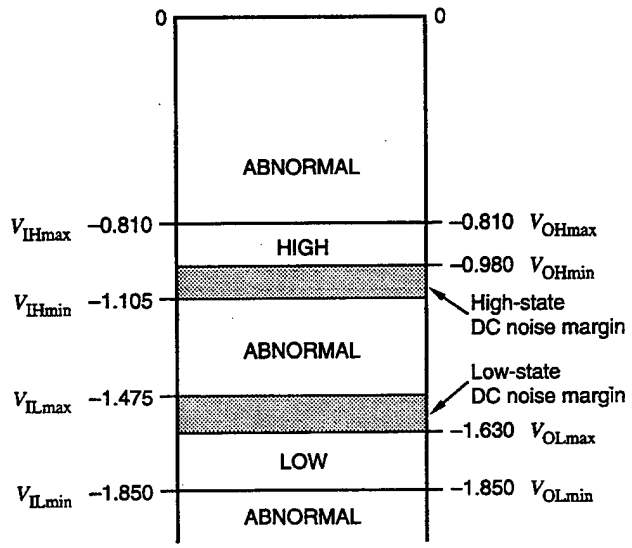


Figure B.3: ECL 10K Family Logic Levels [Reference 21: p. 179].

Figures B.4 and B.5 are circuits of the basic 10K and 10H gates respectively. The 10H family is a higher performance ECL family having gate propagation delays near 1 ns as opposed to the 10K's typical 2 ns propagation delay. Typical ECL gates consist of multiple inputs, a differential amplifier stage, a bias network, and complementary emitter-follower outputs. Most ECL devices include a normal and an inverting output to reduce chip count. Chip densities are generally on the large scale or medium scale integration (LSI or MSI) level since very large scale integration (VLSI) is not a realistic option given the thermal implications. Variations due to ambient temperature appear in the graph of typical ECL transfer characteristics, Figure B.6. DC loading characteristics of a typical ECL gate are found in Reference 19.

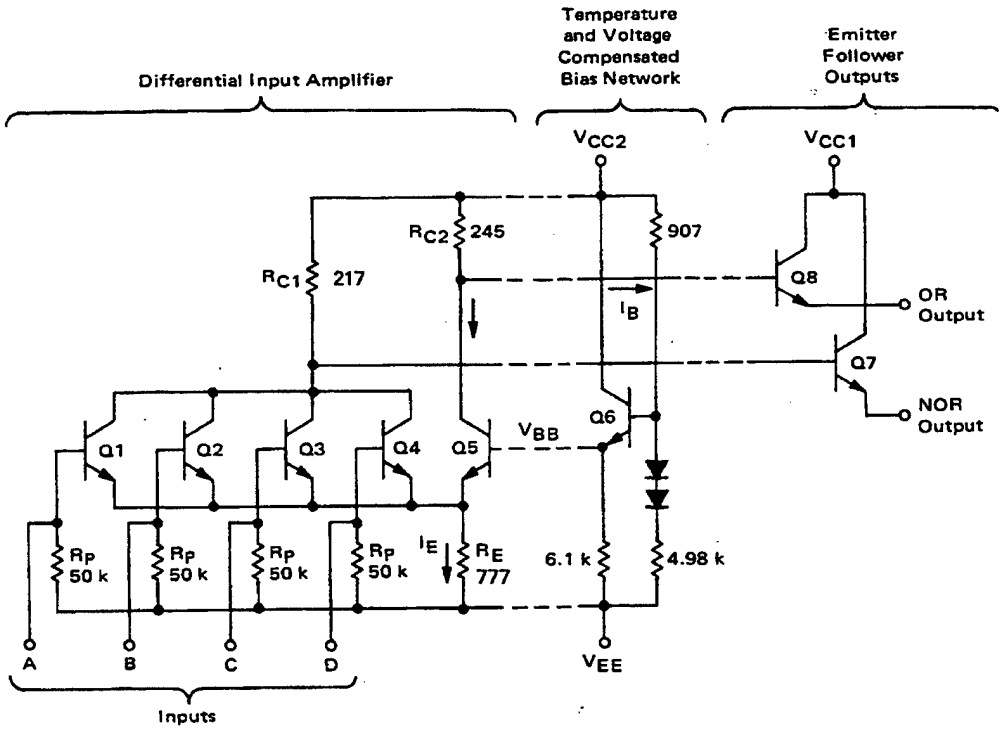


Figure B.4: ECL 10K Circuit Diagram [Reference 19: p. 2].

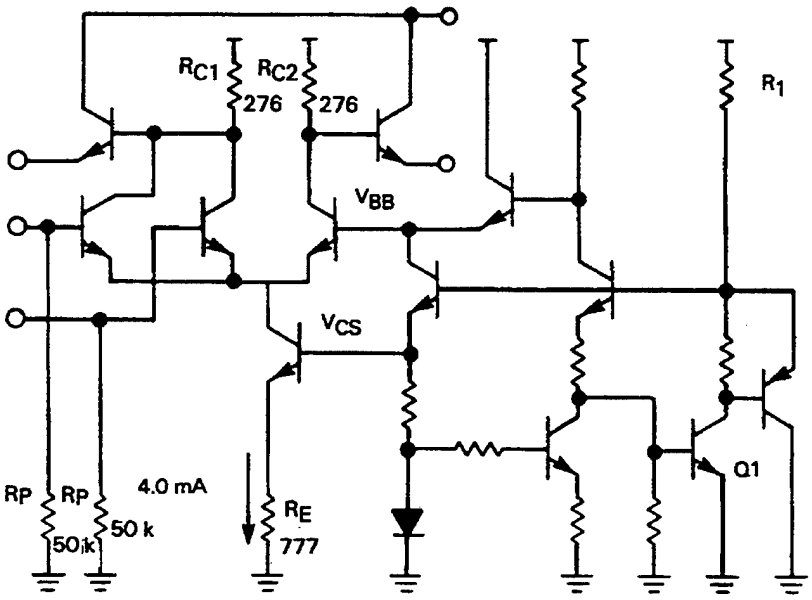


Figure B.5: ECL 10KH Circuit Diagram [Reference 19: p. 1].

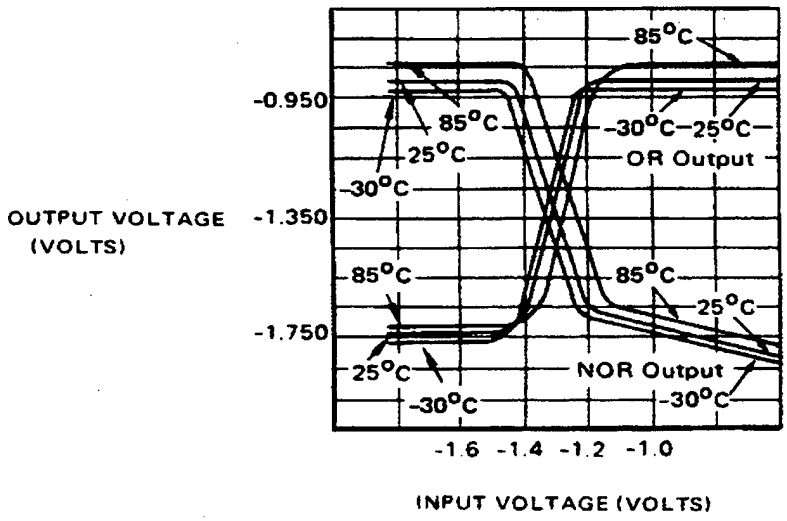


Figure B.6: Typical 10K Transfer Characteristics as a Function of Temperature [Reference 19: p. 5].

Fall time and propagation delay for ECL gates are largely a function of load capacitance and the emitter pull-down resistor. Fall time (t_f) is given in Equation B.1 and propagation delay (t_{pd}) is listed in Equation B.2.

$$t_f \approx (1.1 \cdot RC + 2) \quad ns \tag{B.1}$$

$$t_{pd} \approx (0.47 \cdot RC + 2) \quad ns \tag{B.2}$$

As a signal propagates down a transmission line, the delay will increase due to loading capacitance. Equation B.3 displays the modified propagation delay (t'_{pd}). C_d is capacitance due to loading. C_o is the intrinsic line capacitance.

$$t'_{pd} = t_{pd}\sqrt{1 + C_d / C_o} \tag{B.3}$$

The characteristic impedance of the transmission line due to load capacitance is found in Equation B.4. Z_o is the original characteristic impedance without a load.

$$Z_o' = \frac{Z_o}{\sqrt{1 + C_d / C_o}} \tag{B.4}$$

Signal voltage drop (ΔV_{Sig}) in a line terminated to V_{TT} may be calculated using Equation B.5. R_T is the value of the terminating resistor and V_{OH} is the logic one output voltage. The maximum unterminated line length (ℓ) is calculated by Equation B.6. Rise time is represented by t_r (the time between the 20% to 80% levels). ℓ may be used by the designer to know when series and parallel termination techniques (as described in the next section) are required.

$$\Delta V_{Sig} = \left(\frac{2 - |V_{OH}|}{R_T} \right) \cdot (\text{line resistance}) \tag{B.5}$$

$$\ell_{\max}(in.) = \frac{t_r}{2t'_{pd}} \tag{B.6}$$

3. An ECL Design Primer: Basic Transmission Line Theory

For all but the *shortest* interconnection lines, transmission line effects with high speed ECL circuits must be considered by the digital designer. *Shortest* here means less than six inches for the 10K family and less than two inches for the 100K family. On these short lines, adverse transmission line effects such as ringing, severe overshoot and undershoot, and interference do not occur. In the prototype design, several signal interconnect lines required transmission line design methods to minimize adverse effects. The transmission line may be approximated by the equivalent circuit of a transmission line (Figure B.7) which shows the constant representation of the transmission line's inductive and capacitive effects.

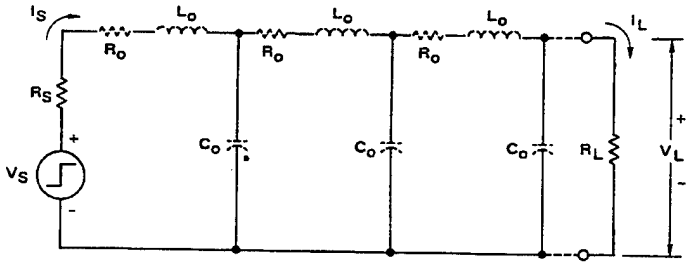


Figure B.7: Equivalent Circuit of a Transmission Line [Reference 19: p. 121].

To reduce adverse transmission line effects, (1) line length may be reduced, (2) ECL devices with slower rise times may be used, (3) series damping at the sending end may be used, (4) parallel damping at the receiving end may be used, and/or (5) matched terminations can be employed. In the prototype data link design, line length was held below the specified limits whenever possible. The 10K family was selected for the prototype design due to the use of wire-wrap methods. A PCB implementation is required to use higher performance families such as 10H or ECLinPS. Pull-down resistors (R_P) to V_{TT} for each ECL output signal were used in this design. Series damping resistors (R_D) of 150 Ω were used to for longer line lengths. Ideally the series damping resistor plus the gate's output characteristic impedance (Z_o) matches the transmission line's characteristic impedance (approximately 150 Ω in the case of the data link prototype). The ECL gates used in the data link design have an approximated $Z_o = 10$ Ω so damping resistors of 140 Ω would improve signal quality. However, the closest resistors available for the prototype during implementation was 150 Ω. Figure B.8 illustrates the termination method used between ECL gates. Also, matched terminations between ECL devices are used whenever possible. Matched terminations are not always possible when interfacing between the 15T/R modules (100K family compatible) and MECL 10K gates. The 15R module requires 300 Ω pull-down resistors to V_{TT} while 10K gates have a maximum output pull-down resistor of 100 Ω to prevent noise margin degradation.

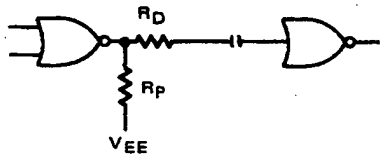


Figure B.8: ECL Termination Method Used in Data Link [Reference 19: p. 27].

APPENDIX C. SUPPORTING EQUIPMENT.

A. POWER SUPPLIES

To insure proper operation of the prototype data link, power supplies capable of meeting the ECL logic and 15 T/R module current requirements must be used. V_{EE} supplies for the transmitter and receiver buses should be connected to power supplies capable of providing –5.2 Vdc at 2 A or greater. V_{CC} supplies for all circuit boards should be capable of providing +5.0 Vdc at 1 A or greater. The +15 V and –15 V supplies required by the ADC may use 0.25 A supplies (0.50 A rated supplies are better). Running the data link circuit boards with supplies operating too close to their maximum current rating may cause unpredictable behavior.

B. 20 MHz FUNCTION GENERATOR

The function generator is used to generate variable analog input signals for the ADC. The Wavetek 20 MHz Pulse/Function Generator is adequate for use with the ADS-944 ADC. It is capable of generating sinusoidal, triangular, square, and pulse analog signals greater than 10 MHz in frequency. Triangular waveforms ranging between +/– 1.25 V were used to generate all ADC binary patterns. Signals begin to break down around 10 MHz in the Wavetek function generator.

C. 200 MHz OSCILLOSCOPE

The Tektronix 2445B 200 MHz oscilloscope was used to monitor signals on the prototype circuit boards during implementation and testing. The 200 MHz scope was used instead of a 100 MHz due to the enhanced resolution provided. Use of grounded signal probes is a must.

D. DIGITAL LOGIC ANALYZER

The Hewlett-Packard 16500B logic analyzer was used to monitor the transmitter and receiver data lines. Data was captured by triggering on the rising edge of the TX and RX STRBOUT signals. TX STRBOUT is used to latch data into the transmitter module. RX STRBOUT latches received data from the receiver module. The logic analyzer may operate data pods in either TTL or ECL mode. For ECL mode, it is essential the triggering clock waveform be a high quality ECL signal. Failure to provide such a clock signal will prevent the logic analyzer from capturing the data correctly.

APPENDIX D. ADS-944 ADC PCB LAYOUT.

Printed circuit board layers for the Datel ADS-944 electronic analog-to-digital converter are included in this appendix.

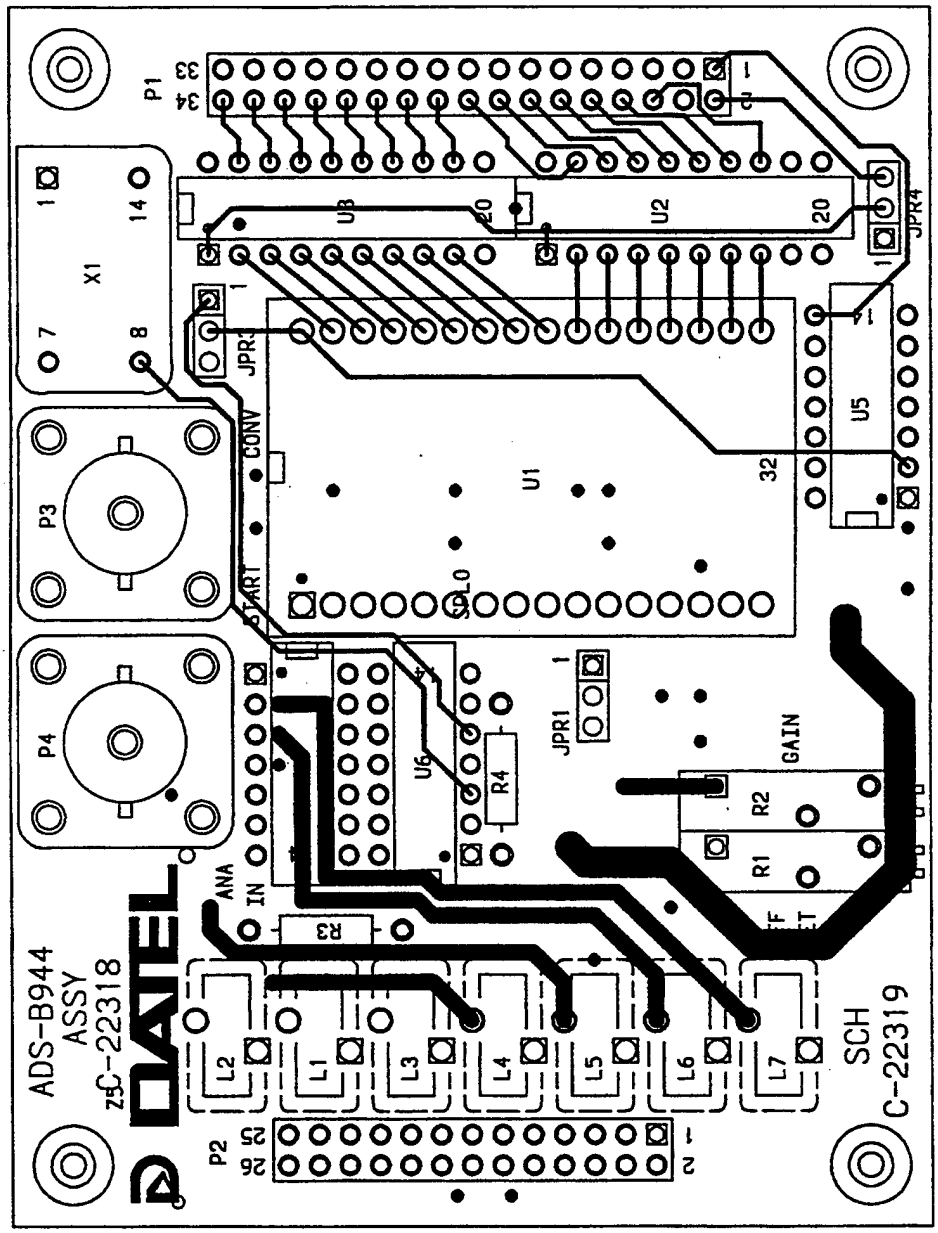


Figure D.1: ADS-944 ADC PCB Layer 1(Datel).

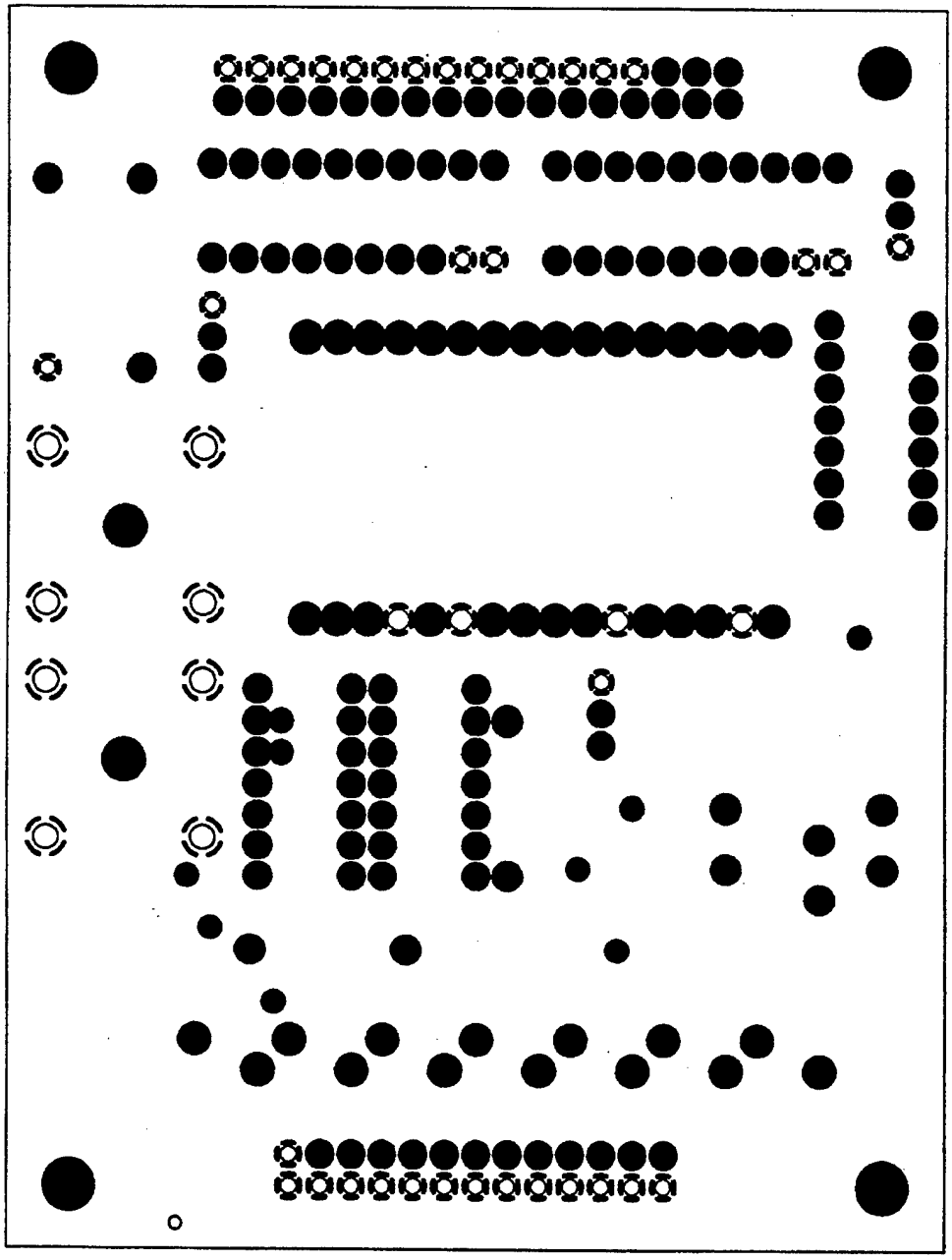


Figure D.2: ADS-944 ADC PCB Layer 2 (Datel).

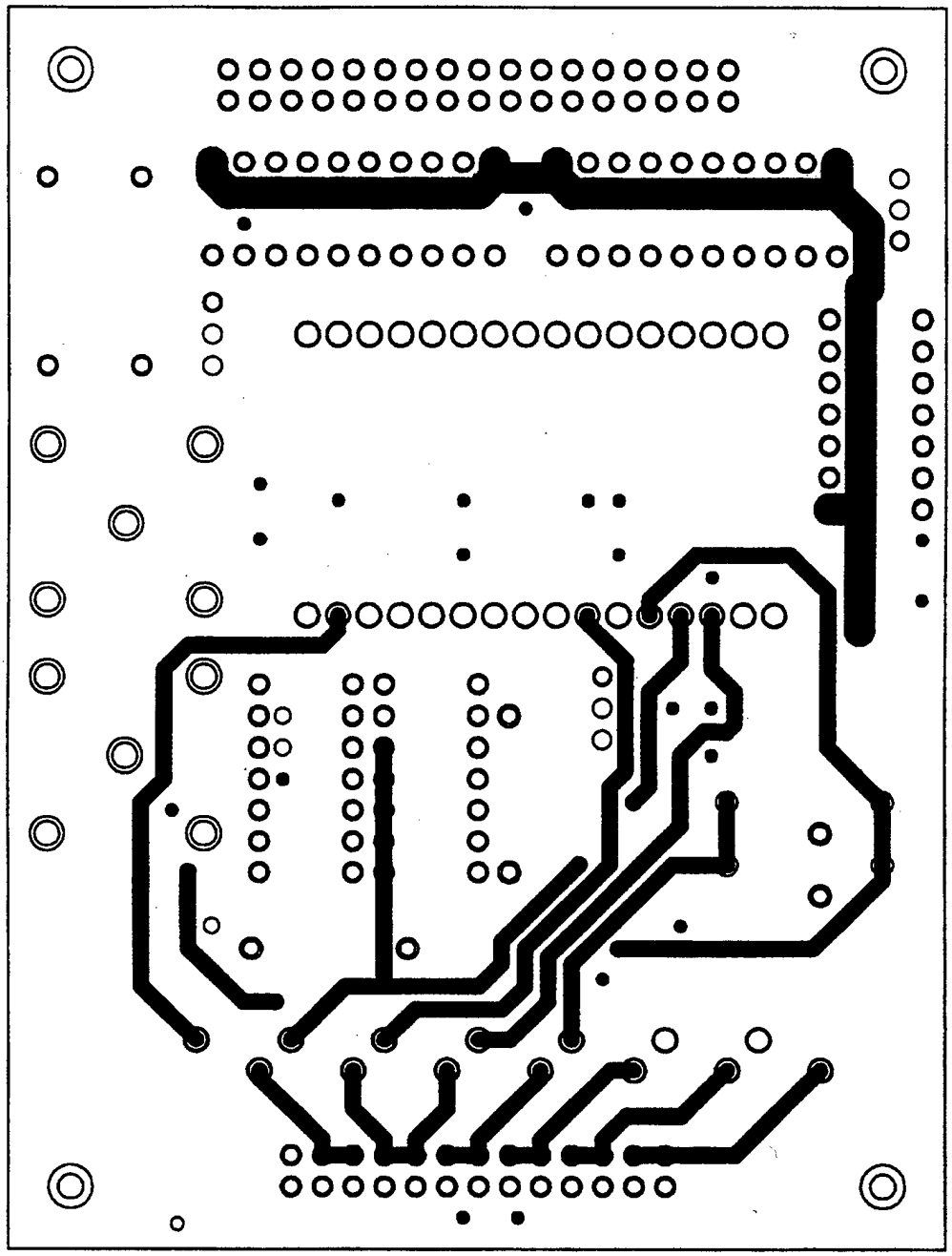


Figure D.3: ADS-944 ADC PCB Layer 3 (Datel).

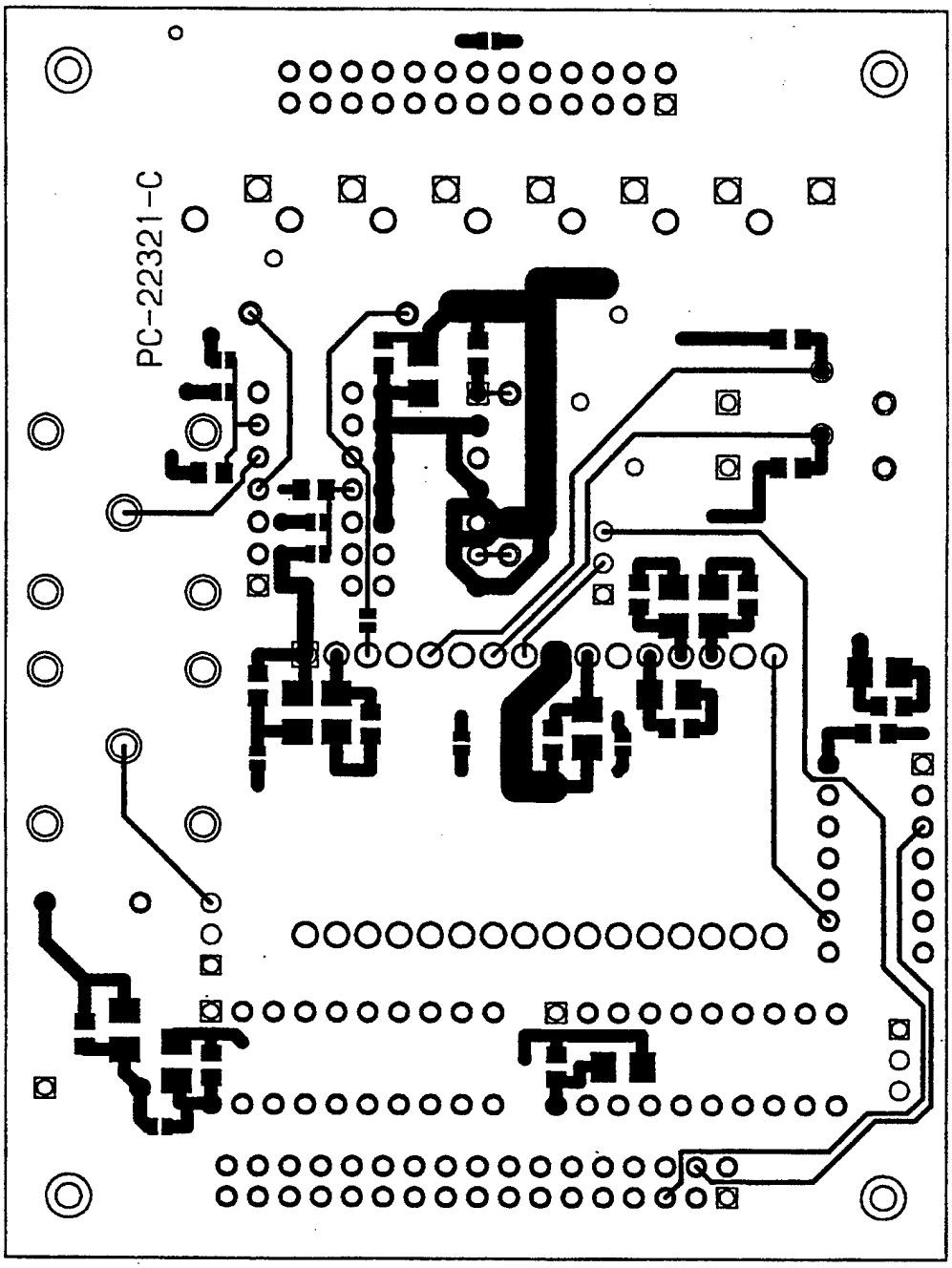


Figure D.4: ADS-944 ADC PCB Layer 4 (Datel).

APPENDIX E. CONVENTIONS USED IN THE DATA LINK DESIGN.

A. DIGITAL LOGIC CONVENTIONS

To aid the reader, this section lists a few conventions used throughout this thesis. Transistor-transistor logic (TTL) devices, as used in the data link design, have two common voltage potentials, V_{CC} and GND. In TTL, V_{CC} denotes a +5.0 Vdc potential and GND refers to digital ground (0 Vdc). The emitter-coupled logic (ECL) components have five common voltage potentials, V_{CC}, V_{EE}, V_{TT}, V_{BB}, and GND. V_{CC}, the most positive voltage supply, is normally 0 Vdc except in TTL-ECL translators where it is +5.0 Vdc. V_{EE}, the most negative supply, is normally –5.2 Vdc. V_{TT}, the pull-down reference potential voltage, is normally –2.0 Vdc. V_{BB}, the bias voltage, is typically –1.3 Vdc. Lastly, GND is the same as the TTL convention, 0 Vdc.

B. OTHER CONVENTIONS

Other conventions include abbreviations used for some of the data link components. ADC (or A/D converter) is used in the literature for analog-to-digital converter. Unless otherwise stated, ADC refers to an electronic analog-to-digital converter. TX denotes the electro-optic transmitter while RX refers to the electro-optic receiver.

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